AN ANALYSIS OF THE RESPONSE OF DIGITAL DEMODULATORS TO FREQUENCY SHIFT KEYED SIGNALS

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THESIS

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TO FREQUENCY SHIFT KEYED SIGNALS

by

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The theory and operational characteristics of a digital pulse counting frequency demodulator are presented. The demodulator, called the pulse width demodulator (PWD) in this report, is realized with solid state components and uses pulse circuitry to perform demodulation. The output of the demodulator may be applied to a low pass filter (LPF) to recover the modulating voltage.

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(20. ABSTRACT Continued)

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The demodulator performance for analog and digital (FSK) modulating voltages is obtained at both commercial intermediate frequencies of 455 kHz and 10.7 MHz. Its performance in the presence of noise is investigated and compared to theoretical results for non-coherent FSK systems.

An Analysis of the Response of Digital Demodulators to Frequency Shift Keyed Signals

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I. INTRODUCTION

Frequency demodulators convert the instantaneous frequency of the incoming or intermediate frequency (IF) signal to a voltage. Analog frequency demodulators use phase-sensitive or frequency-sensitive circuitry to convert frequency to voltage. One configuration is the phase-locked loop. Other realizations, such as the Foster-Seely discriminators, ratio detectors and differentiating techniques, produce a bandpass signal whose envelope is proportional to the instantaneous frequency. Ordinary envelope detectors then recover the modulation.

It has been known for some time that digital methods can be used to demodulate FM carriers since the information is contained in the zero crossings of the carrier. Early digital frequency demodulators were called boxcar detectors and are described by Terman [Ref. 1]. More recently, similar devices called cycle-counting discriminators or pulse rate discriminators are treated extensively in the literature [Refs. 2, 3, 4, and 5].

With the advent of reliable and easy to use digital integrated circuits capable of relatively high frequency (10 MHz) operation, digital methods of frequency demodulation are receiving closer scrutiny [Refs. 2, 3, 4 and 5]. Application of these devices in the area of frequency measurement, demodulation of broadband signals and in commercial radios

is now possible. Nearly all present applications of digital frequency demodulators use the cycle counting technique.

In this report the response of a digital demodulator to analog and digital modulating signals is presented. In each instance the results are obtained for the important case involving additive noise. The investigative tool is a digital demodulator of simple design using standard integrated circuit (IC) components. While initially considered a new pulse counting demodulator, subsequent analysis revealed its close similarity to the well known cycle counting demodulator. Nevertheless, its usefulness for the conduct of this investigation was evident and the resultant data is deemed generally applicable to pulse counting demodulators irrespective of individual circuit realization.

II. NATURE OF THE PROBLEM

With the availability of digital circuit components which perform well at higher frequencies (10 - 15 MHz) the possibility of cycle counting discriminators as frequency demodulators is promising. For example, the digital devices find application in commercial stereo receivers and laboratory instrumentation [Ref. 3]. This study considers the performance of a digital demodulator with analog and digital (FSK) modulating voltages and in the presence of additive noise.

An initial consideration was to conduct an investigation of the response to FSK signals of the well known cycle counting demodulator [Ref. 2]. However, early work involved the design and fabrication of a digital demodulator using NAND gates. The resultant device, called the Pulse Width Demodulator (PWD) in this report, was used throughout the study.

Initially it was thought the PWD constitutes a "new" frequency demodulator; however, the derivation of the demodulator characteristic indicates a close relationship to the well known cycle counting demodulator. The similarity of the two demodulators is discussed later in this report.

The performance of the PWD was observed at 10.7 MHz IF and at 455 kHz IF. The demodulator was also used to recover a binary data bit stream in the frequency shift keyed (FSK)

mode. To complete the analysis, noise was introduced to both the analog and digital signals and the demodulator performance noted.

The demodulator achieves good analog signal recovery at both commercial intermediate frequencies. With additive noise, a SN ratio of 9.5 dB results in a recovered audio signal with a barely noticeable noise level, while a SNR of 5 dB results in the recovery of a still intelligible voice signal accompanied by annoying noise.

With FSK signals, error rates for various SNRs of the input signal are measured and compared to the appropriate theoretical curves of probability of error versus SNR for a non coherent FSK system. The laboratory results agree with theoretical predictions.

The demodulator functions consistently, without changing any of its circuit values, over the entire frequency range of operation. In addition to the primary frequency range of operation there exist other ranges of operation at higher frequencies. Operation at higher frequencies is possible because the PWD automatically performs frequency division when input frequencies are even multiples of the maximum frequency in the primary range of operation. Thus adjusting the demodulator for an operating range from 0-1 MHz will cause the demodulator to function at 2-3 MHz, 4-5 MHz, etc.

The initial adjustment for operation over a desired frequency range also determines the demodulator sensitivity,

which then remains constant. The highest sensitivity is obtained when operating in the first frequency range of operation. Proceeding into the second and third, etc., operating ranges reduces the sensitivity by a factor of two for each transition.

The investigation shows that practical pulse counting demodulators are easily constructed from currently available components. They are rugged and reliable. They require only one screwdriver adjustment as preparation for operation. This adjustment is not critical and does not require subsequent readjustments. They are capable of good performance with both analog and digital modulating voltages. Furthermore, they offer many advantages not available with many analog demodulators such as asynchronous operation, insensitivity to changes in carrier frequency (local oscillator drift), linear characteristic over a broad bandwidth, operation over several frequency ranges for a single adjustment, and economy of construction.

III. THEORY AND PERFORMANCE

A. THEORY

1. The Pulse Counting Demodulator (PCD)

The PCD is a digital demodulator of very simple design. It is discussed extensively in the literature [Ref. 2] and is found in commercial as well as laboratory applications [Ref. 3]. Fig. 1 shows the block diagram of a PCD.

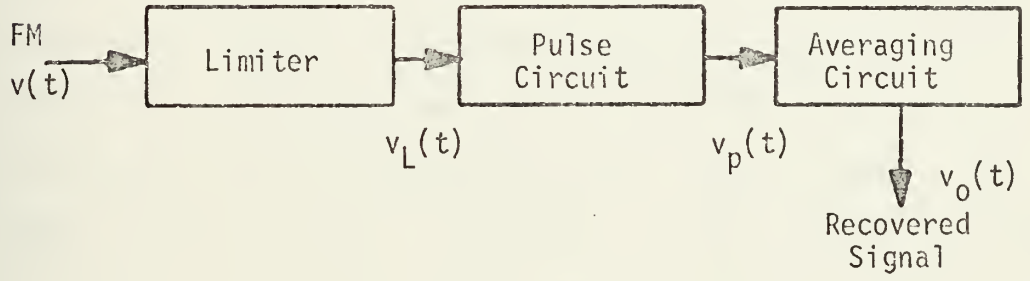


Fig. 1. Block Diagram of a Pulse Counting Demodulator (PCD)

The circuit functions by generating a pulse of constant amplitude and constant duration for each cycle of the input signal. The input is a frequency modulated signal which may be expressed as:

$$v(t) = A \cos \left(w_c t + \Delta f \int_0^t m(t)\, dt\right) \qquad (1)$$

where

A = signal amplitude

w_c = carrier frequency

Δf = peak carrier frequency deviation

$m(t)$ = modulating voltage

This signal is hard limited to form $v_L(t)$ which is used to trigger the pulse circuit. The output of the pulse circuit is a series of identical pulses (constant width, constant amplitude) which are spaced according to the frequency of the input signal. Averaging the output pulses (a low pass filter may be used) results in a voltage proportional to the instantaneous frequency of the input signal. Fig. 2 shows pictorially how the output voltage level is obtained by dividing the area of the pulse by the period of the incoming frequency. From Fig. 2 the output voltage $v_o(t)$ is given as:

$$v_o(t) = V_p\tau/T = V_p\tau f_i \qquad f_i \leq 1/\tau \tag{2}$$

where

f_i = $1/T$ = instantaneous frequency of $v(t)$ (3)

V_p = pulse amplitude

τ = pulse duration

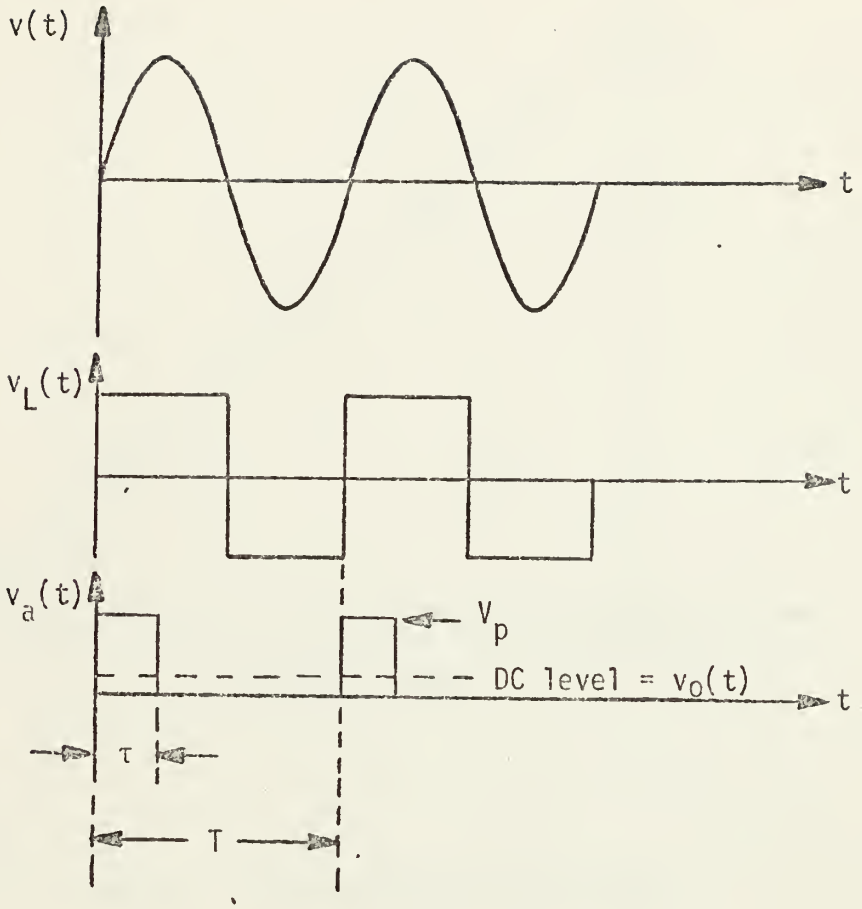


Fig. 2. Waveforms Associated with Fig. 1.

Equation (2) indicates that the "per cycle DC level" of $v_a(t)$, which is the usable output $v_o(t)$, is linearly dependent on the instantaneous frequency f_i of the input signal since both τ and V_p are constants. A plot of $v_o(t)$ vs. f_i is the discriminator characteristic and is shown as Fig. 3. Note that the output voltage varies linearly with frequency as is desired for frequency demodulation.

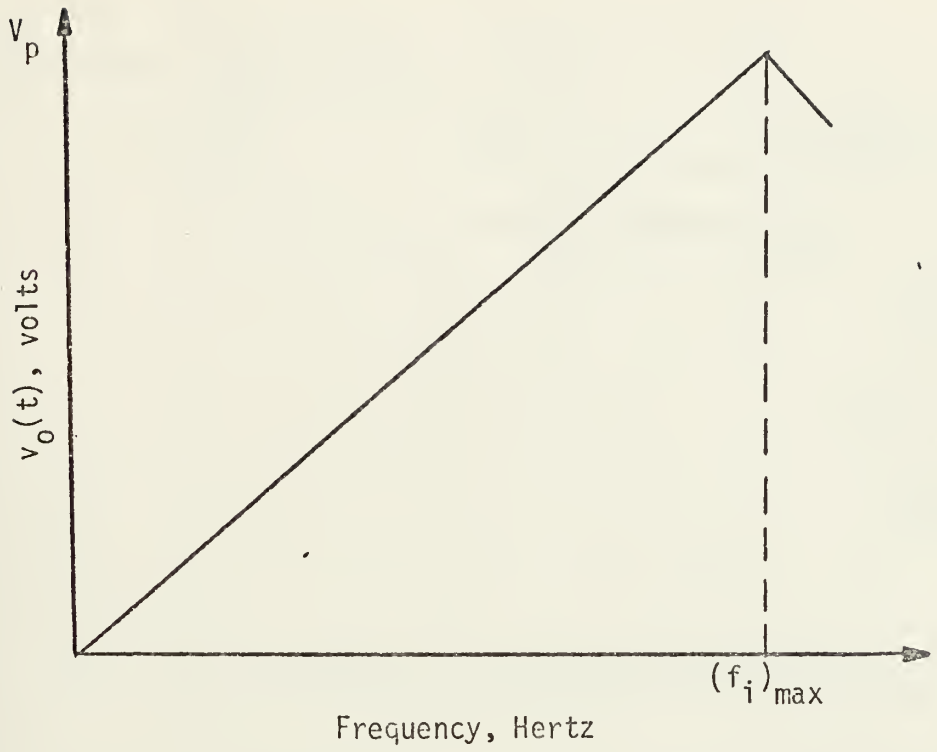


Fig. 3. The PCD Characteristic

2. The Pulse Width Demodulator (PWD)

The digital frequency demodulator used throughout this investigation is presented in Fig. 4. Its basis of operation is the comparison of a hard limited input signal with an internally generated reference pulse of constant duration. The resultant waveform is averaged to again produce the "per cycle DC level" proportional to the instantaneous frequency of the input signal.

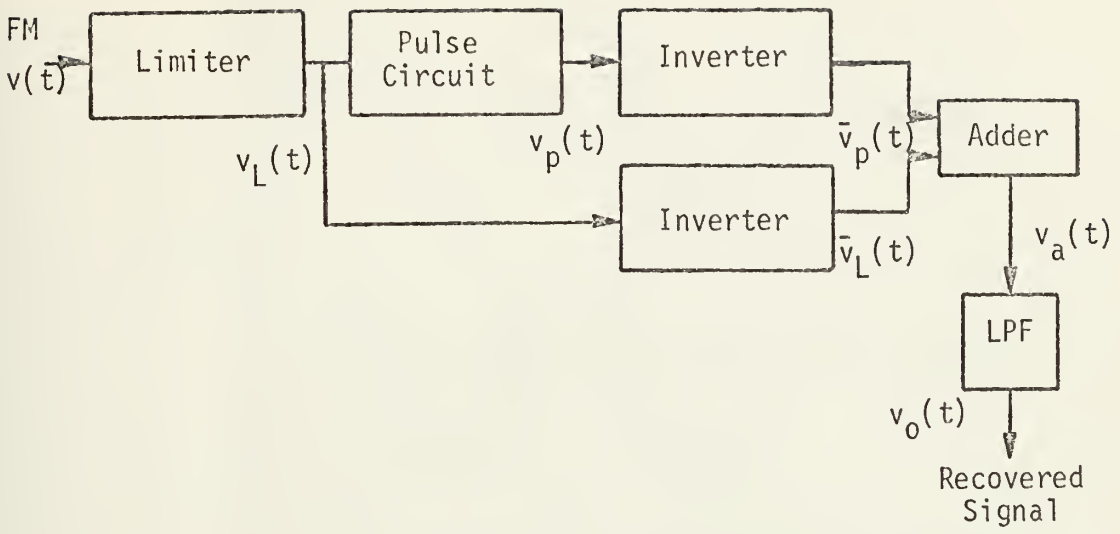


Fig. 4. The Pulse Width Demodulator (PWD)

Fig. 5 shows the appropriate waveforms for the PWD. The PWD output voltage $v_o(t)$ is proportional to the average value of $v_a(t)$. From Fig. 5, $v_o(t)$ is given as,

$$v_o(t) = v_p\left(\frac{1}{2} + \frac{\tau}{T}\right) \qquad \tau = \frac{1}{2(f_i)_{max}} \leq \frac{T}{2} \qquad (4)$$

$$v_o(t) = v_p\left(\frac{1}{2} + \tau f_i\right) \qquad (5)$$

This "time varying DC level" is plotted versus f_i as Fig. 6. As for the case of the PCD, $v_o(t)$ is seen to be a linear function of f_i of the input signal.

Equation (5) is important in several respects because it describes the demodulator operation. It provides information

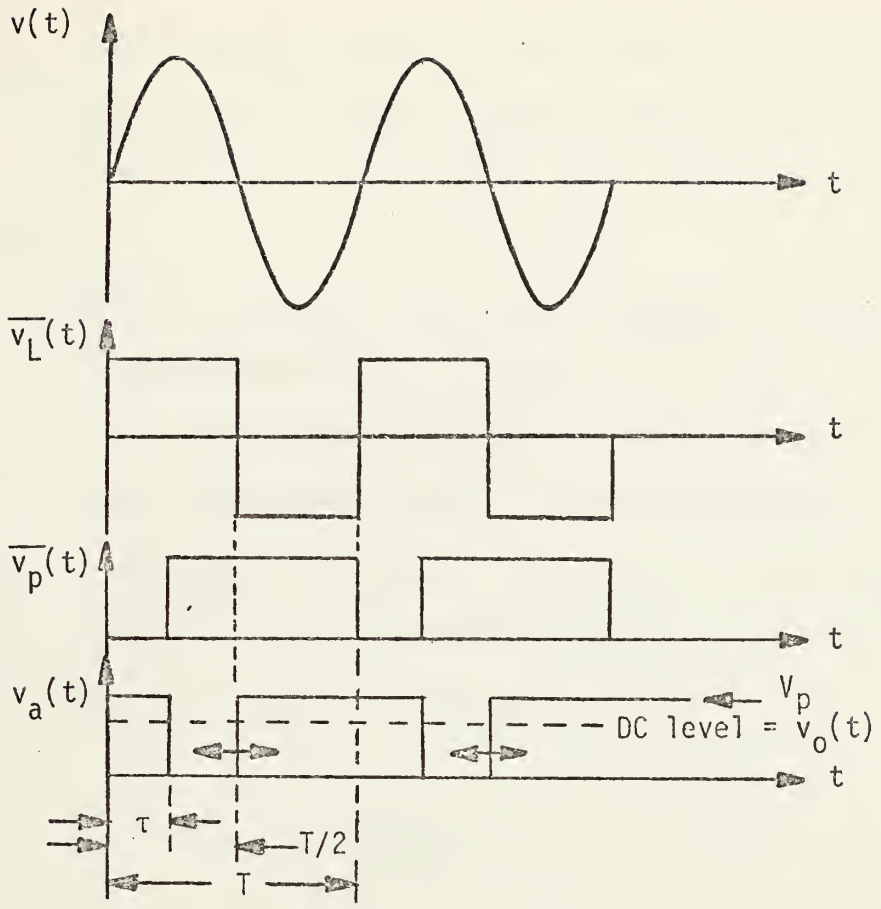


FIG. 5. WAVEFORMS ASSOCIATED WITH FIG. 4

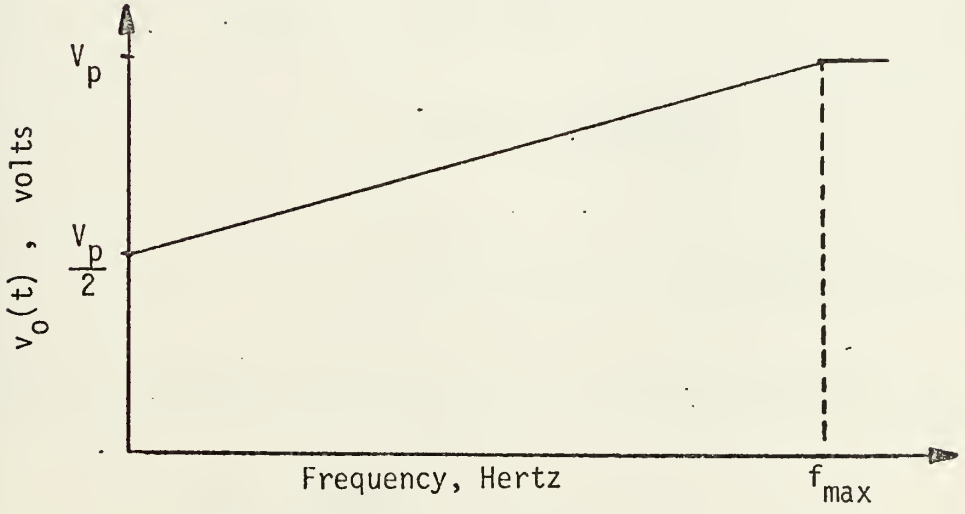


FIG. 6. PWD CHARACTERISTIC

concerning the frequency range of operation, the DC voltage recoverable over that frequency range and the relationship between the reference pulse width τ and the instantaneous frequency f_i.

Equation (5) states that the frequency range of operation for the demodulator is from $f_i = 0$ to $f_i = 1/2\tau = (f_i)_{max}$. It is clear that $(f_i)_{max}$ may be varied to suit the particular requirements by varying the pulse width τ. The selection of a frequency range of operation is based on knowledge of carrier peak frequency deviation Δf and is controlled by the reference pulse width τ as:

$$\tau = \frac{1}{2(f_i)_{max}} \tag{6}$$

where

$$(f_i)_{max} = f_c + \Delta f \tag{7}$$

f_c = carrier frequency

Δf = peak carrier frequency deviation

From Fig. 6 the PWD sensitivity S in volts per Hertz is

$$S = \frac{(V_p - V_p/2)}{(f_i)_{max}} = (V_p/2)(2\tau) = V_p\tau \tag{8}$$

Since V_p is a constant for a given demodulator circuit, the sensitivity S is a function of the operating frequency range, which for all practical purposes extends from $f_i = 0$ to $f_i = (f_i)_{max} = \frac{1}{2\tau}$.

Using equation (8), a plot of the demodulator sensitivity S versus maximum frequency $(f_i)_{max}$ is possible and is shown as Fig. 7. It is pointed out that the product of S and $(f_i)_{max}$ is a constant anywhere along the curve.

By viewing one cycle of $v_a(t)$ on an oscilloscope, it is possible to observe the instantaneous frequency of an applied signal v(t). The window of $v_a(t)$ in the interval $(\tau, T/2)$ opens as the frequency decreases and closes as the frequency increases.

3. PCD and PWD Equivalence

Equations (2) and (5) relate the PCD and PWD. The respective transfer functions differ only by a constant. In practice the difference depends on the actual circuit realization; however, one difference is the operating frequency ranges obtained for identical adjustments of the reference pulse width. Fig. 8 shows the theoretical transfer characteristic of both demodulators using 4 volt circuitry and adjustment for operation in the 0-250 kHz frequency range. Note that the sensitivity S is the same for each. The difference in the operating ranges is due to the ability of the pulse forming circuit of the PCD to function with a duty cycle factor which is greater than 0.5.

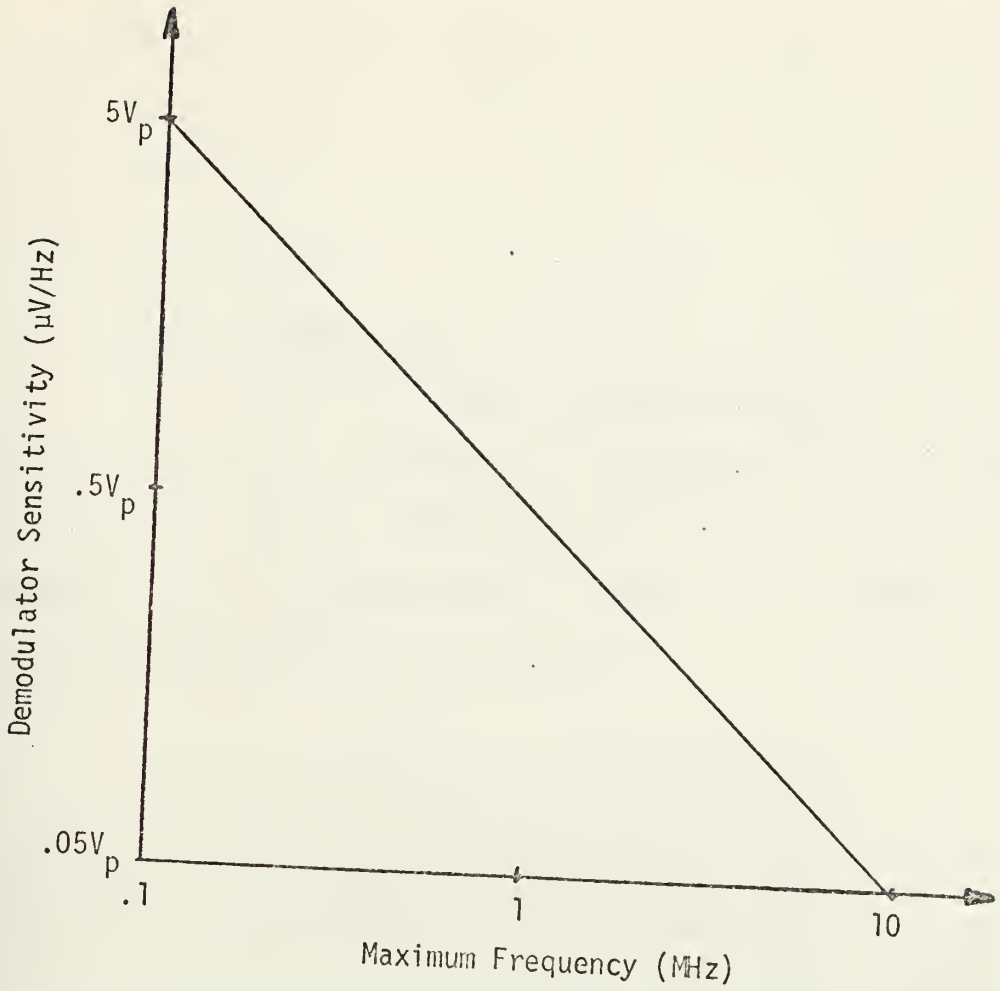


FIG. 7. SENSITIVITY S VS. MAXIMUM FREQUENCY $(f_i)_{max}$

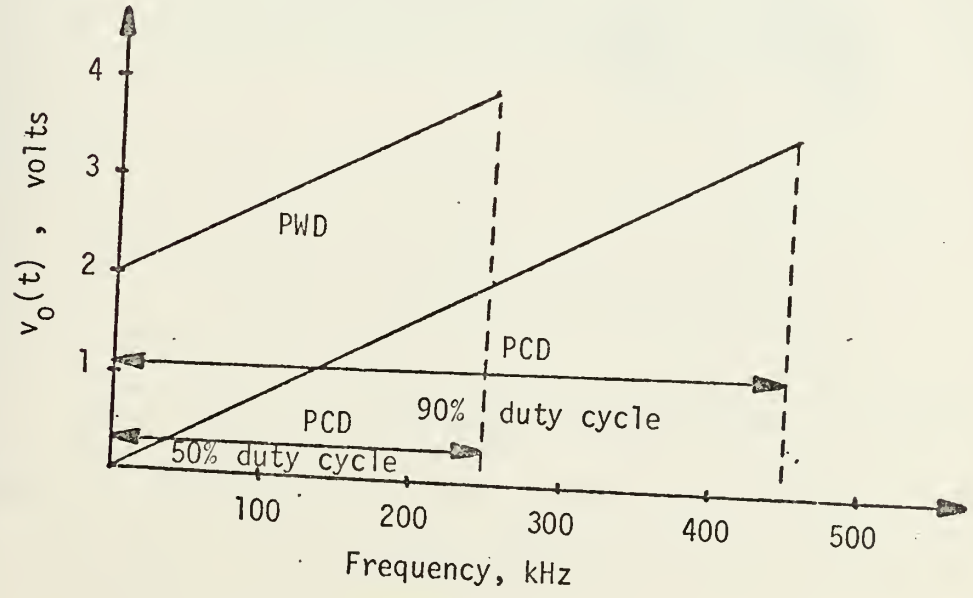


FIG. 8. AN EXAMPLE OF THE PWD AND PCD CHARACTERISTICS

The remainder of this report deals with the PWD; however, the findings are generally applicable to all pulse counting demodulators.

B. CIRCUIT REALIZATION

1. Circuit Components

Fig. 4 shows the block diagram of the PWD. In realizing the block diagram it is necessary to use pulse circuits which operate reliably and accurately enough at frequencies up to approximately 11 MHz. The circuit eventually realized is shown in Fig. 9.

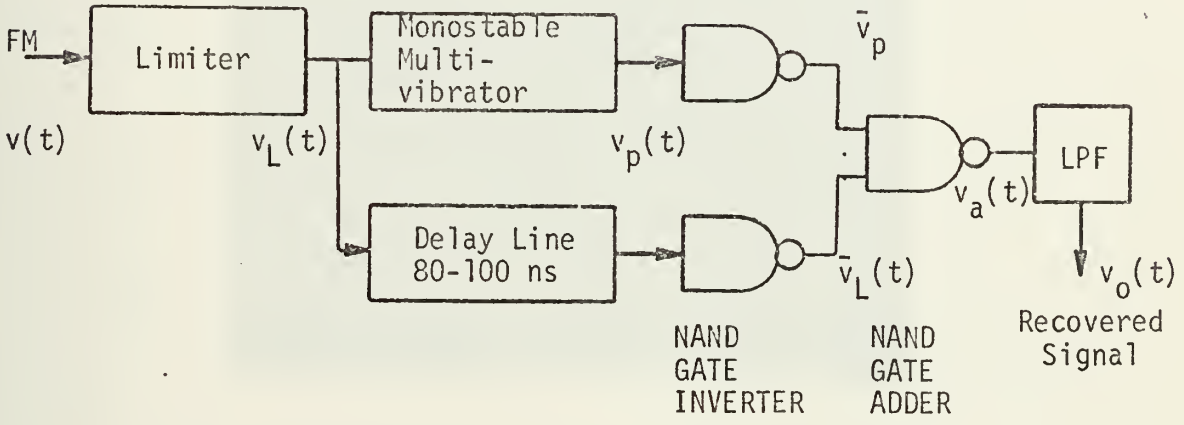


FIG. 9. BLOCK DIAGRAM OF PWD

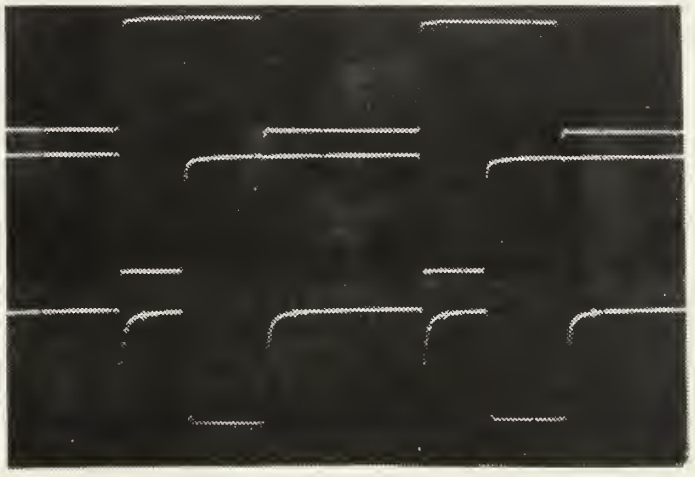
The limiter is designed using 2N3404 transistors to produce a sufficiently strong signal to trigger the monostable multivibrator. To achieve this goal it is necessary to drive

the limiter using a 12 volt power supply. All other circuit components require a 5 volt supply and produce 4 volt pulses. Appendix A shows the schematic diagrams of all circuits used in this investigation. Appendix A, Fig. 1 shows the schematic diagram of the hard limiter. All components with the exception of the limiter function well up to approximately 10 MHz at which frequency rise times become noticable. The limiter operation begins to deteriorate at approximately 8 MHz, but is still usable at an IF of 10.7 MHz.

(a)

(b)

(c)



(a) and (b) NAND gate adder input waveforms.
(c) The result of NAND gate addition showing "glitches" whose width indicates a time separation of the two signals to be added

FIG. 10. NAND GATE ADDITION FOR TWO PULSE WAVEFORMS WITH DIFFERENT ARRIVAL TIMES AT THE ADDER

The delay line indicated in Fig. 9 is necessary only for operation at high frequencies (10.7 MHz). At this frequency

the time difference for signal propagation between the two paths is approximately equal to the reference pulse width (100 nsec). It is therefore necessary to insure that both signals arrive at the NAND gate within a few nanoseconds of each other. The delay was obtained by using eight NAND gates in series since each NAND gate possesses a propagation delay of approximately 12-20 nsec. Appendix A, Fig. 2 shows the schematic of the PWD and the delay line.

At lower frequencies the delay line is unnecessary although the effects of its absence are observable on the oscilloscope. Fig. 10 is a photograph showing the effects of different propagation times on the addition of two signals at the NAND gate.

2. NAND Gate Addition

Comparison of $\overline{v_L}$ with the generated reference pulse $\overline{v_p}$ takes place at the NAND gate adder. The bar over v_L and v_p indicates the inversion of the respective signal. Thus if v_L is a positive pulse which goes from 0 to 5 volts, then $\overline{v_L}$ is a pulse which goes from 5 volts to 0 volts. NAND gate logic is shown below.

$$\begin{array}{ccccc} 1 & + & 0 & = & 1 \\ 0 & + & 1 & = & 1 \\ 0 & + & 0 & = & 1 \\ 1 & + & 1 & = & 0 \end{array}$$

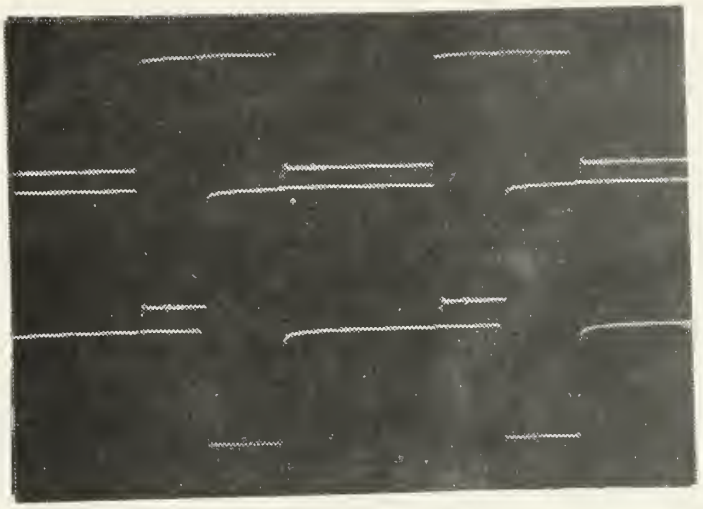
The output of the NAND gate is a pulse waveform containing information relating the instantaneous frequency

separation between the incoming signal and the reference pulse. Fig. 11 (a) is a photograph of NAND gate addition of a limited input signal ($\overline{v_L}$ of Fig. 5) and the reference pulse ($\overline{v_p}$ of Fig. 5). The resultant waveform $v_a(t)$ of Fig. 5 is also shown. Fig. 11 (b) shows the same addition for the case of the input signal frequency being equal to the maximum frequency $(f_i)_{max}$.

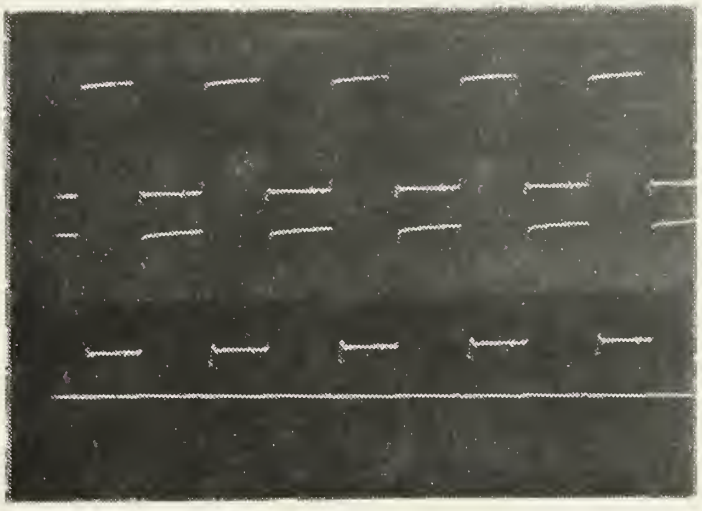
C. PERFORMANCE

1. Linearity

To test the PWD characteristic for linearity (the variation of its output voltage as a function of instantaneous frequency), the circuit of Fig. 4 was constructed and tested. Initially the pulse producing network is adjusted for generating a .33 usec pulse. This adjustment sets the maximum frequency at 1.5 MHz. The discriminator is then swept with frequencies up to the maximum frequency and the curve of Fig. 12 is thus obtained. The theoretical curve for a 4 volt pulse circuit is also provided for comparison. The actual curve is seen to be quite linear, deviating from the theoretical curve primarily at the low frequencies. It should be remembered that this curve is valid for 4 volt pulse circuits. Substitution of 4 volt for V_p in equation (5) results in v_{out} taking on the value of two volts at zero frequency and four volts at the maximum frequency, as predicted by theory.



(a) $f_i < (f_i)_{max}$ Top and center waveforms are the inputs to the NAND gate adder. The bottom waveform is the adder output $v_a(t)$.



(b) $f_i = (f_i)_{max}$ Note that the output of the NAND gate adder $v_a(t)$ (bottom waveform) is a DC level.

FIG. 11. NAND GATE ADDITION

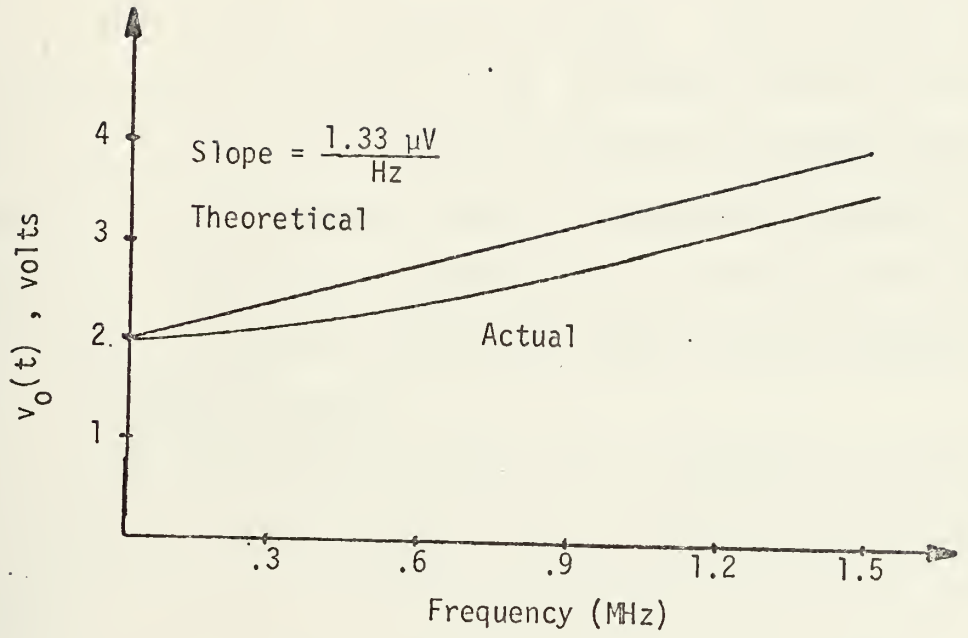


FIG. 12. PWD OUTPUT VOLTAGE VS. FREQUENCY FOR THE CASE OF A 1.5 MHz MAXIMUM FREQUENCY

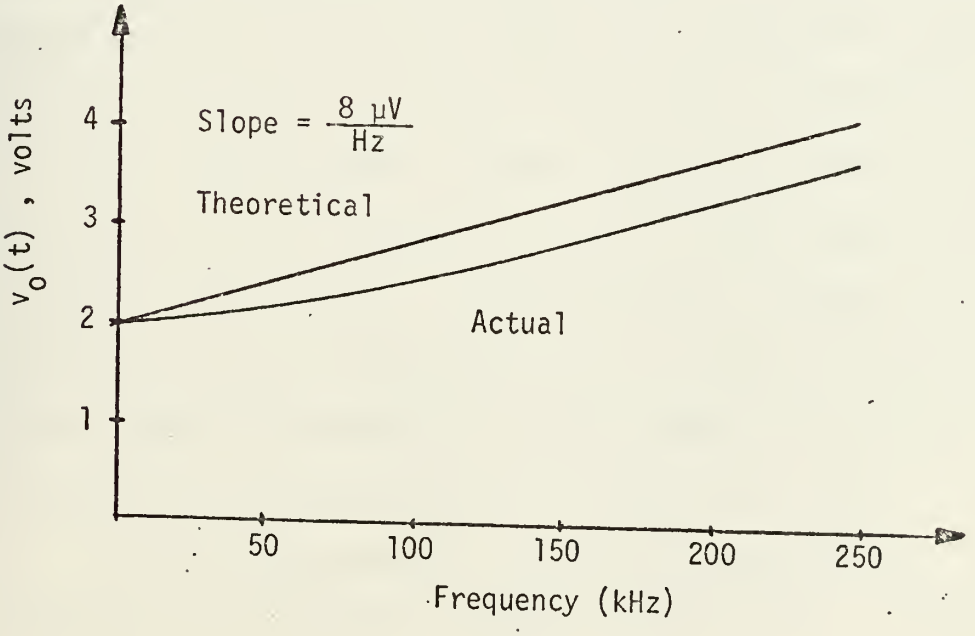


FIG. 13. PWD OUTPUT VOLTAGE VS. FREQUENCY FOR THE CASE OF A 250 kHz MAXIMUM FREQUENCY

To test for the linearity of circuit operation at other frequencies, the reference pulse width is readjusted for a lower maximum frequency and the output voltage versus frequency curve obtained. Fig. 13 shows the new curve. Once again it is seen that the circuit is quite linear throughout its frequency range. The small departure from linearity at the lower frequencies is caused by the inability of the LPF to operate well over such a large frequency range.

2. Operating Ranges

Equation (5) describes the demodulator output voltage as a function of frequency. For convenience it is reproduced below:

$$v_o(t) = V_p(\frac{1}{2} + \tau f_i) \qquad f_i \leq \frac{1}{2\tau}$$

This equation describes circuit operation only up to the maximum frequency at which point the demodulator ceases to function and seems to remain inoperative indefinitely. This is not the case however, because laboratory work and the waveforms of Fig. 5 indicate that when the input frequency is greater than $2(f_i)_{max}$ the demodulator resumes operation. Increasing the input frequency still further discloses yet another range of operation beyond a range of no-operation. All operating and non-operating ranges are equal.

Fig. 14 depicts the situation graphically. It represents the frequency division pictorially. Frequency

division is performed by the pulse forming circuit. When the frequency of the applied signal exceeds $(f_i)_{max}$, the pulse forming network is being triggered while it is in the process of forming a pulse. It thus ignores the second trigger pulse. Since the trigger is the limited input wave, the circuit in effect ignores every other cycle of v(t) thus performing frequency division by two. At even higher frequencies, every third cycle causes triggering, etc.

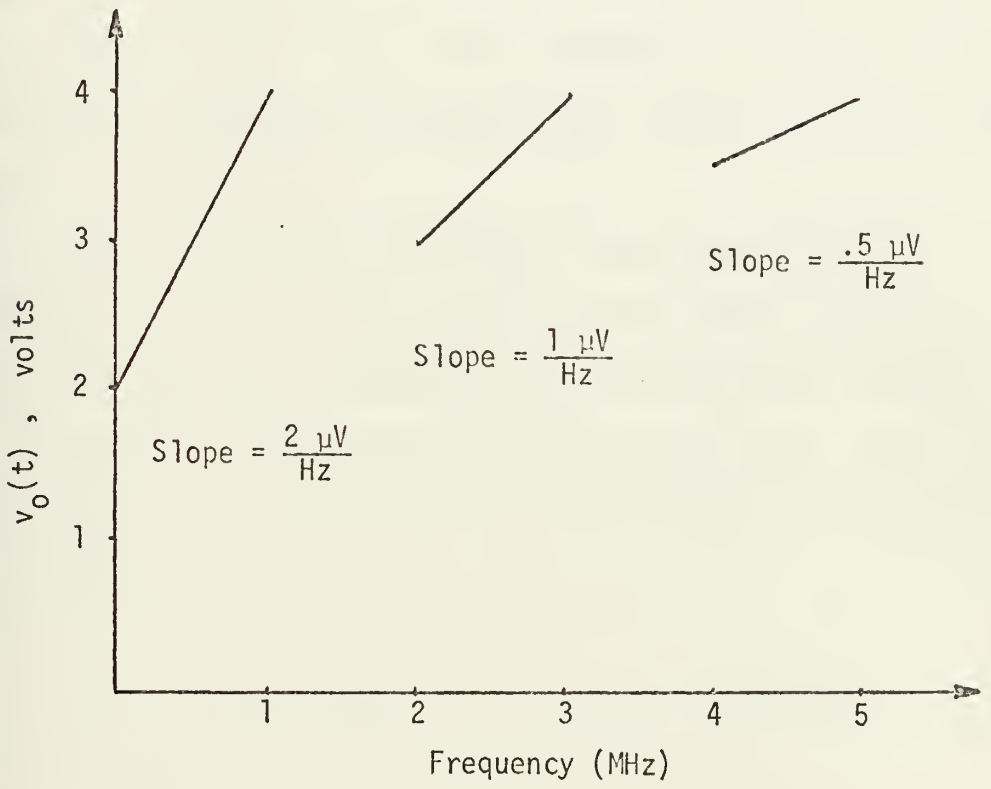


FIG. 14. PWD OUTPUT VOLTAGE VS FREQUENCY SHOWING HIGHER FREQUENCY RANGES OF OPERATION

3. Sensitivity

It has been shown that the demodulator output voltage per each cycle of frequency deviation (demodulator sensitivity S) for a given circuit realization is determined by $(f_i)_{max}$ for which the demodulator is adjusted. See Equ. (8). Once this adjustment is made the demodulator sensitivity remains constant over the total operating range. The slopes of Figs. 12 and 13 represent the demodulator sensitivities for the respective maximum frequencies (1.5 MHz and 250 kHz). These sensitivities could have been obtained from Fig. 7, the theoretical demodulator sensitivity versus maximum frequency curve.

When frequency division occurs, sensitivity is reduced as shown in Fig. 14. At each higher operating range of frequency, sensitivity is reduced by a factor of two compared to the preceding operating range. The sensitivity S_n of the nth frequency range relative to the first may be expressed as:

$$S_n = S_1 \left(\frac{1}{2^n}\right) \qquad n = 1,2,.... \qquad (9)$$

4. Adjustments for Optimum Operation

The general design approach is to operate the PWD in the first frequency range. This means that frequency division should be avoided since frequency division results in reduced demodulator sensitivity. Frequency division is

prevented by adjusting the reference pulse width to the maximum duration permitted by the expected maximum frequency. In other words the adjustment is made as dictated by Eq. (6). This pulse duration will result in the highest discriminator sensitivity possible for the given operating frequency range without frequency division. Obtaining this condition is very important since the recovered signal amplitude is the product of the demodulator sensitivity and the frequency deviation. Since frequency deviation is fixed, efforts are made to optimize the sensitivity S. If this is not done the recovered signal amplitude may be too small to be of any use. Thus the demodulator output $v_o(t)$ is represented as:

$$v_o(t) = (S)\ (\Delta f) \qquad (10)$$

As an example consider the case of demodulating a signal at the commercial AM IF of 455 kHz with a frequency deviation of 10 kHz. If first a 0.1 usec pulse is selected, the discriminator sensitivity becomes 0.1 uV/Hz and the recovered signal amplitude is

$$v_o(t) = (S)\ (\Delta f)$$

$$= (0.1\mu V/Hz)\ (10\ kHz)$$

$$= 1\ mV$$

Here and in the rest of this section we have set V_p = 1 volt. This rather weak signal is the result of adjusting the circuit for high frequency operation and proceeding to use it at low frequencies. For a 0.1 μsec reference pulse, the maximum frequency is 5 MHz. Obviously the discriminator is improperly adjusted for operation at 455 kHz.

Consider now a reference pulse of 1 μsec. The resultant sensitivity is 1 μV/Hz and the recovered signal amplitude is now 10 mV, a substantial improvement.

$$v_o(t) = (1\ \mu V/Hz)\ (10\ kHz)$$

$$= 10\ mV$$

For this case the maximum frequency is 500 kHz. Since the frequency deviation is 10 kHz, the reference pulse may be adjusted to obtain a maximum frequency of 460 kHz (455 kHz ± 5 kHz). The reference pulse width for this case is 1.08 μsec and the recovered signal amplitude is 10.8 mV. Obviously the reference pulse width setting is not exceedingly critical to the circuit operation. It is only necessary that it be adjusted accurately enough to place the demodulator operation into a desired frequency range and to make the concomitant maximum frequency sufficiently greater than the sum of the carrier frequency and the peak frequency deviation to provide a small margin of safety.

Operation utilizing frequency division may be desirable (especially at high frequencies) since it permits the use of wider reference pulses (smaller frequency ranges). Wider reference pulses result in higher demodulator sensitivity even after sensitivity reduction due to frequency division. See Table I for examples of this.

Table I shows the respective operating ranges and sensitivities for several reference pulse widths. A point of interest concerning operation in the frequency division mode is evident. It is seen that operation at the commercial AM intermediate frequency IF of 455 kHz with a reference pulse of 1 μsec recovers a 10 mV signal. Operation at the same frequency using a 2.5 μsec reference pulse and with frequency division by two recovers a 12.5 mV signal. This example points out the necessity of calculating the amplitude of the recovered signal for each prospective reference pulse to determine which pulse width results in a larger recovered signal.

5. Analog Signals

a. Without Noise

It is desirable to observe the demodulator performance with analog modulating signals. To perform this analysis, the system of Fig. 15 is used. A 455 kHz carrier is obtained from a function generator whose output is frequency modulated by an audio signal. The amplitude of the audio modulating signal is properly attenuated to produce

TABLE I

OPERATING PARAMETERS OF THE PWD FOR VARIOUS REFERENCE PULSE WIDTHS
(V_p set = 1 volt)

PULSE WIDTH (μsec)	OPERATING RANGE	SENSITIVITY (μV/Hz)	RECOVERED SIGNAL AMPLITUDE (mV)
.1	0 to 5. MHz	.1	1.0 (AM)
	10 MHz to 15. MHz	.05	7.5 (FM)
.2	0 to 2.5 MHz	.2	2.0 (AM)
	5 MHz to 7.5 MHz	.1	
	10 MHz to 12.5 MHz	.05	7.5 (FM)
.4	0 to 1.25 MHz	.4	4.0 (AM)
	2.5 MHz to 3.75 MHz	.2	
	5.0 MHz to 6.25 MHz	.1	
	7.5 MHz to 8.75 MHz	.05	
	10 MHz to 11.25 MHz	.025	3.75(FM)
.5	0 to 1.0 MHz	.5	5.0 (AM)
	2 MHz to 3 MHz	.25	
	4 MHz to 5 MHz	.125	
	6 MHz to 7 MHz	.0625	
	8 MHz to 9 MHz	.031	
	10 MHz to 11 MHz	.015	2.25(FM)
.8	0 to 625 MHz	.8	8.0 (AM)
	1.25MHz to 1.87 MHz	.4	
	2.5 MHz to 3.12 MHz	.2	
	3.75MHz to 4.37 MHz	.1	
1.0	0 to 500 kHz	1.0	10.0 (AM)
	1 MHz to 1.5 MHz	.5	
	2 MHz to 2.5 MHz	.25	
1.5	0 to 333 kHz	1.5	
	666 kHz to 1 MHz	.75	
2.0	0 to 250 kHz	2.0	
	500 kHz to 750 kHz	1.0	
2.5	0 to 200 kHz	2.5	
	400 kHz to 600 kHz	1.25	12.5 (AM)
4.0	0 to 125 kHz	4.0	
	250 kHz to 375 kHz	2.0	10.0 (AM)
	500 kHz to 625 kHz	1.0	

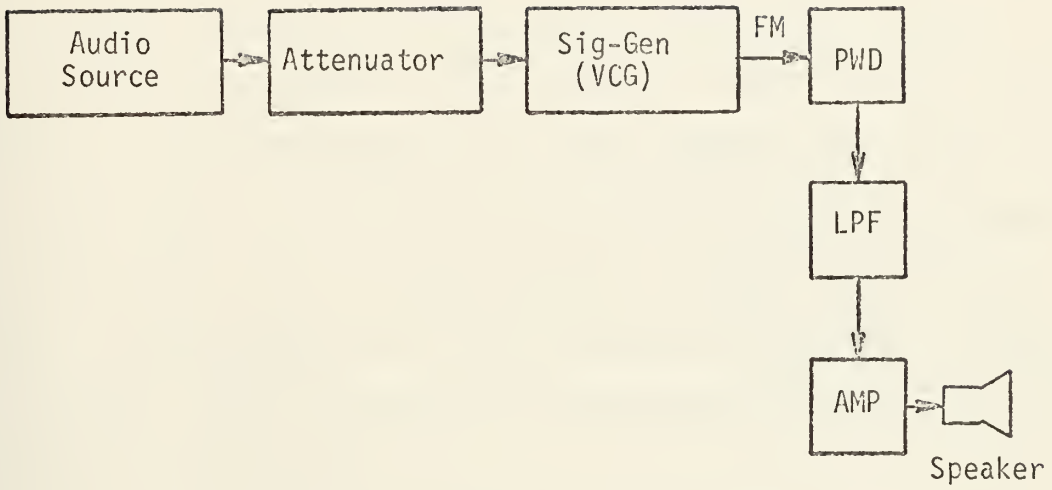


FIG. 15. BLOCK DIAGRAM OF THE SYSTEM USED TO OBSERVE THE RECOVERY OF ANALOG MODULATING SIGNALS

the desired frequency deviation of ± 5 kHz. The frequency modulated signal is then applied to the PWD and the recovered signal amplified and applied to a speaker. The schematic diagram of the 50 dB amplifier is found in Appendix A, Fig. 3.

To prepare the PWD for operation at 455 kHz requires setting the reference pulse to a width of approximately one microsecond. The maximum frequency that can be discriminated is now set at 500 kHz. For the case at hand, since the center frequency is 455 kHz and the deviation is

± 5 kHz, the highest frequency anticipated is 460 kHz, well below the maximum frequency. Should the input frequency exceed 500 kHz, distortion results (demodulation ceases and the recovered voltage is a DC level). With the PWD adjusted for a 1.0 μsec reference pulse, the demodulator sensitivity is 4 μV/Hz and the anticipated recovered signal is computed to be 40 mV. Here we have used the circuit value of $V_p = 4$ volts. The demodulator is now properly adjusted for operation at 455 kHz. When operating, it produces a clear sound (no detectable distortion).

To determine if the full 10 kHz deviation is required for good recovery of the audio signal, the modulating signal is attenuated to produce smaller and smaller frequency deviations from the center frequency. In all other respects the block diagram of Fig. 15 remains the same. It is anticipated that as the frequency deviation is reduced the recovered signal will grow progressively fainter until only the circuit noise remains. The results of this test are as expected and are summarized in Table II.

The effect of a varying carrier frequency is investigated simply by controlling the output frequency of the function generator. Varying the carrier frequency has no effect on the demodulator performance. The PWD continues to produce a clear signal with no change in volume. Caution had to be exercised, however, to insure that the carrier frequency was not increased to such a level which resulted

TABLE II

EFFECT OF FREQUENCY DEVIATION ON RECOVERED AUDIO

Frequency Deviation	Recovered Audio
10.0 kHz	Loud and Clear
6.4 kHz	Normal and Clear
3.0 kHz	Soft and Clear
1.4 kHz	Soft and Clear
800 Hz	Very Soft and Clear
400 Hz	Very Soft and Clear
less than 400 Hz	Inaudible

in a frequency exceeding the maximum frequency. The total range over which the carrier frequency was varied is quite impressive; being 10 kHz to 500 kHz. Below 10 kHz the recovered signal is accompanied by a shrill whistle. At approximately 3 kHz the distortion is so severe that the signal is not discernible.

The PWD is now adjusted for operation at 10.7 MHz. The frequency deviation is ± 75 kHz (commercial FM). The identical circuit configuration of Fig. 15 is used. The only PWD adjustment required is the setting of the reference pulse width τ to 0.1 μsec. Referring to Table I, it is seen that several pulse widths can be selected and still achieve effective demodulation. Whatever setting is selected, it is seen that frequency division is a normal mode of operation. Again , V_p = 4 volts is used. In spite of frequency division by two, the recovered signal is quite strong (30 mV). If a

0.2 μsec pulse is selected, the demodulator performs frequency division by three and again the recovered signal is 30 mV. It is seen from Table I that these two settings of the reference pulse are optimum for operation at this frequency. To further increase the quality of the demodulator performance at 10.7 MHz, a delay line is placed in the path of the limited input signal. This delay line ensures the simultaneous arrival at the NAND gate of both signals.

As in the case of operation at 455 kHz, the PWD recovers a clean audio signal at 10.7 MHz. The demodulator continues to function as the carrier frequency is varied between 10 MHz and 11 MHz.

Table I does not include data for pulse durations less than 0.1 μsec. Smaller pulse widths can be used in theory. For example, use of a 0.04 μsec reference pulse width would eliminate frequency division by placing 10.7 MHz into the first operating frequency range in which case the recovered signal is 24 mV. The primary difficulty in using such narrow pulses occurs at the NAND gate where the pulses are compared. Comparison of pulses is done most easily with pulses whose width is greater than the propagation delay times of the circuit. For example, the circuits comprising the PWD have propagation delays which range from 10 nsec to 100 nsec. Obviously any circuit designed to handle pulses of duration comparable to the circuit delay times must compensate for or eliminate such effects. The need for compensation may be avoided by using larger reference pulse widths.

b. Carrier Plus Noise

All carrier with additive noise analysis is performed at 455 kHz only. The system shown in Fig. 15 is modified to allow the addition of noise to the frequency modulated signal prior to its being applied to the PWD. Fig. 16 shows the system configuration used for the audio with additive noise analysis. A schematic diagram of the summing amplifier is found in Appendix A, Fig. 5. This configuration performs very poorly when noise is added to the signal. A signal to noise ratio (SNR) of approximately 18 dB is required to produce a usable output. An analysis of the waveforms at various points in the system suggests a solution which when implemented results in satisfactory performance.

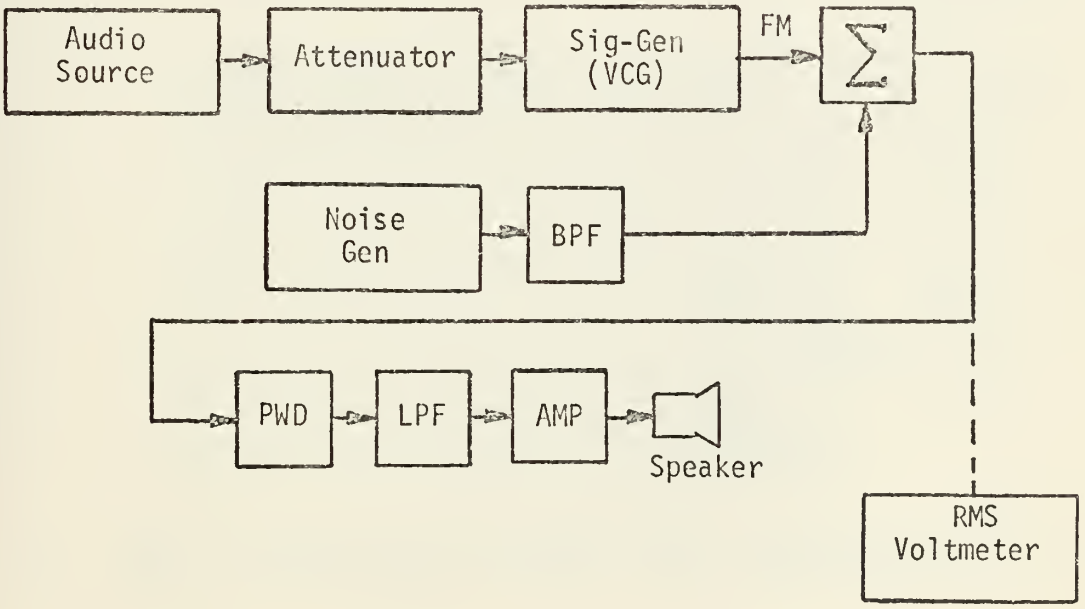


FIG. 16. BLOCK DIAGRAM OF THE SYSTEM USED TO OBSERVE THE RECOVERY OF AN ANALOG MODULATING SIGNAL WITH ADDITIVE NOISE

The solution implemented to reduce the demodulator vulnerability to noise consists of following the summing amplifier by a saturating amplifier the output of which is used to trigger a Schmitt trigger. Appendix A, Fig. 6 shows the schematic diagram of the saturating amplifier and Schmitt trigger. Improved performance is achieved by the Schmitt trigger which fires only if a certain threshold is exceeded by the input signal. The saturating amplifier is necessary to insure consistent firing of the Schmitt trigger. The modified system is shown as Fig. 17.

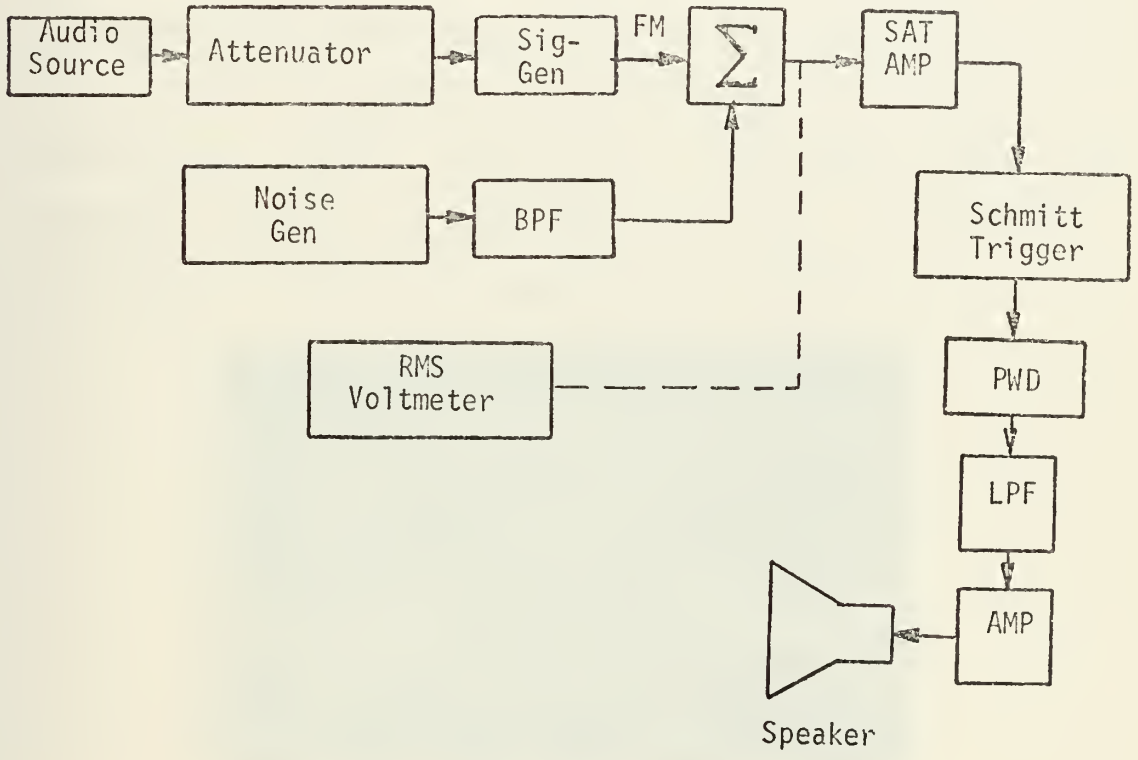
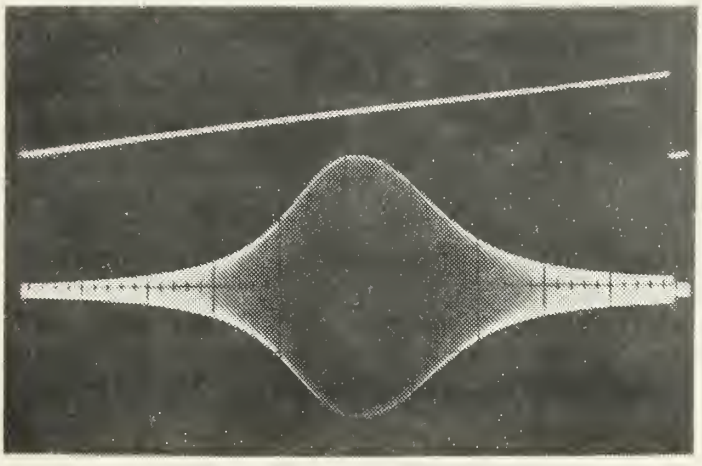


FIG. 17. FIG. 16 MODIFIED TO REDUCE THE VULNERABILITY OF THE PWD TO NOISE

Considerable improvement in system performance results. The SNR required for no discernible noise is 10.75 dB whereas an SNR of 9.48 dB produces an audio accompanied by a barely discernible noise. At a SNR of 5 dB speech is discernible but accompanied by loud, annoying noise. Finally, at a SNR of just under 4 dB no audio signal is discernible.

The SNR is measured at the output of the summing amplifier where the input signals are the band filtered noise and the frequency modulated signal. The noise generator produces wideband white noise assumed to be Gaussian. The noise is band filtered to give a 10 kHz bandwidth centered at 455 kHz. Actually the filter bandwidth is nearly five to seven times greater. Fig. 18 is a photograph showing the frequency response of the band pass filter. The 3 dB bandwidth is seen to be approximately 54 kHz.



300 kHz 455 kHz 600 kHz

FIG. 18. THE FREQUENCY RESPONSE OF A BAND-PASS FILTER (BPF) USED FOR THE PWD NOISE ANALYSIS. The upper trace is the voltage applied to the frequency modulator whose output was applied to the BPF.

Fig. 19 (a) through (e) depict a series of photographs showing signal waveforms at the input and output of the summing amplifier, saturating amplifier and the Schmitt Trigger. Waveform (a) is the frequency modulated input to the summing amplifier. Noise is applied to the other input terminal of the summing amplifier. Waveform (b) is the resultant noise-contaminated amplifier output. The output of the saturating amplifier is waveform (c). Waveforms (d) and (e) are the Schmitt Trigger outputs with and without noise respectively.

Table III is a summary of the audio-noise analysis. This table includes the author's subjective comments as to the quality of the recovered audio signal. The rms values of the signal with and without noise are measured at the output of the summing amplifier by a rms voltmeter. Computation of the respective signal to noise ratios is as follows:

Represent $v_o(t)$ as:

$$v_o(t) = s(t) + n(t) \qquad (11)$$

where

$s(t)$ is the frequency modulated signal at the summing amplifier output, and

$n(t)$ is the noise at the summing amplifier output.

(a)

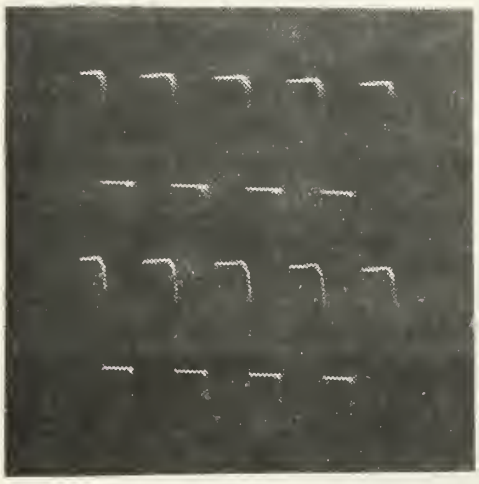
(b)

(c)

(a) Frequency modulated input to the summing amplifier.
(b) Noise contaminated output of the summing amplifier.
(c) Saturating amplifier output.

(d)

(e)



(d) Schmitt trigger output with noise.
(e) Schmitt trigger output without noise.

FIG. 19. SUMMING AMPLIFIER, SATURATING AMPLIFIER AND SCHMITT TRIGGER WAVEFORMS

TABLE III

EFFECT OF THE SIGNAL TO NOISE RATIO OF THE INPUT FM SIGNAL ON THE QUALITY OF THE RECOVERED AUDIO

Center Frequency	Frequency Deviation	LPF Setting	SNR (dB)	Sound Quality
455 kHz	8 kHz	2 kHz	3.5	Loud noise, no signal
455 kHz	8 kHz	2 kHz	5.0	Loud noise, signal audible
455 kHz	8 kHz	2 kHz	6.4	Annoying noise, signal audible
455 kHz	8 kHz	2 kHz	7.7	Low annoying noise
455 kHz	8 kHz	2 kHz	8.5	Noticeable noise
455 kHz	8 kHz	2 kHz	9.5	Barely noticeable noise
455 kHz	8 kHz	2 kHz	10.7	No discernible noise
455 kHz	8 kHz	2 kHz	12.6	No discernible noise

Squaring $v_o(t)$ and averaging gives:

$$\overline{v_o^2(t)} = \overline{[s(t) + n(t)]^2} \qquad (12)$$

$$= \overline{s^2(t)} + \overline{2s(t)n(t)} + \overline{n^2(t)} \qquad (13)$$

Because of the assumed statistical independence of the signal and noise, the second term of Equ. (13) is assumed to be zero. Equ. (12) becomes:

$$\overline{v_o^2(t)} = \overline{s^2(t)} + \overline{n^2(t)} \qquad (14)$$

since

$$(v_o)_{rms} = [\overline{v_o^2(t)}]^{1/2} = [\overline{s^2(t) + n^2(t)}]^{1/2} \qquad (15)$$

On the RMS Meter, we measure $[s^2(t)]^{1/2}$ and $[n^2(t)]^{1/2}$. Therefore the signal to noise ratio (SNR) is obtained as follows:

$$SNR = 10 \text{ Log } \frac{\overline{s^2(t)}}{\overline{n^2(t)}} = 10 \text{ Log } \frac{\overline{s^2(t)}}{\overline{v_o^2(t)} - \overline{s^2(t)}} \qquad (16)$$

6. Digital Signals (FSK)

a. Without Noise

To conduct this part of the analysis, it is necessary to generate a Frequency Shift Keyed (FSK) signal, apply it to the demodulator and compare the recovered signal with the modulating waveform. Figure 20 shows the block diagram of a system which performs this operation. The confirmation of good operation is made by observing the degree of similarity of the waveforms on the oscilloscope.

It is now possible to observe the various properties of the PWD by appropriately modifying the FSK waveform. To understand the specific aspects of the PWD

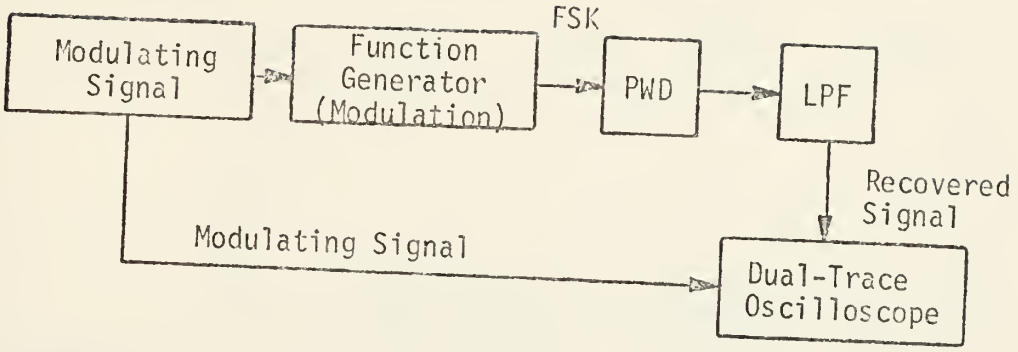


FIG. 20. BLOCK DIAGRAM OF THE SYSTEM USED TO ANALYZE THE PERFORMANCE OF THE PWD WITH A DIGITAL (FSK) INPUT

operation it is necessary to present the system of Fig. 20 in more detail. Figure 21 shows all the components of the system used to analyze the PWD with digital signal inputs. To facilitate the comparison of the recovered and the modulating signals, a shaping circuit has been added to the system of Fig. 21. The wave shaping circuit is actually a zero crossing detector. It purpose is to transform the recovered signal into a pulse waveform of proper amplitude to make the comparison with the modulating waveform easier. The schematic diagram of the shaping circuit is shown in Appendix A, Fig. 4.

In generating the FSK signal, the output of the square wave generator is used to modulate the function generator. The output of the function generator is a FSK signal which may be expressed as:

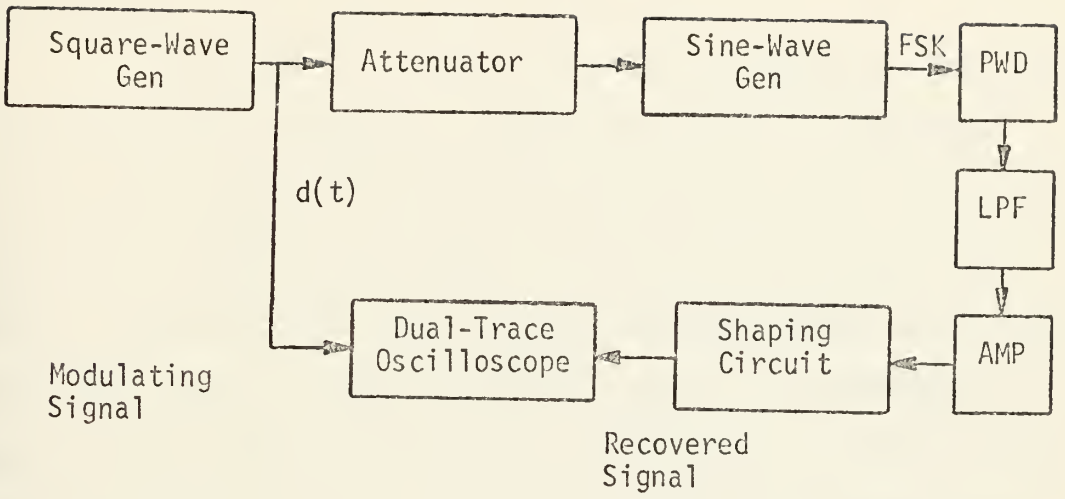


FIG. 21. A MORE DETAILED PRESENTATION OF FIG. 20

$$s(t) = \begin{cases} A \cos 2\pi f_1 t & d(t) < 0 \\ A \cos 2\pi f_2 t & d(t) > 0 \end{cases} \qquad (18)$$

The frequency separation between f_1 and f_2 is a function of the amplitude of the square wave applied to the sine wave generator while the number of cycles in each burst of frequencies f_1 and f_2 depends on the frequency of the square wave. The center frequency, or carrier, about which f_1 and f_2 are spaced is a dial adjustment of the function generator. It is seen that both the carrier frequency and the data rate (square wave frequency) are easily controlled. The bandwidth of the FSK signal is also a function of the amplitude of the

modulating square wave and is controlled by an attenuator which follows the square wave generator.

To allow for the wide range of data rates to be used during the analysis an adjustable LPF is selected. In all cases observed, the limiting factor for recovering the square wave modulating signal is the LPF. The LPF has to be properly selected for each maximum frequency and data rate. Generally, the LPF upper frequency cutoff is adjusted to approximately 25% of the carrier frequency to reduce high frequency terms in the output, while still allowing the recovery of a strong output. As an example, consider the case of a 500 kHz maximum frequency mode of operation. The optimum setting of the LPF, for the noise free case, is approximately 100 kHz. Under these conditions, the recovered signal is a square wave with appreciable rise times. The possible data rates for various LPF upper frequencies are shown in Fig. 22. Figure 22 reflects the properties of the LPF used in this analysis. The filter, A Krohn-Hite bandpass filter model 310-C, provided unity gain and an attenuation of approximately 70 dB per decade. The use of other filters would alter somewhat the curve of Fig. 22. Figure 23 shows the effect on the recovered signal of a constant LPF upper frequency but an increasing data rate. Note that as the data rate increases the LPF becomes the limiting factor in the system and severely attenuates the recovered signal. Figure 24 shows the effect on the recovered signal of an increasing LPF upper frequency. Note that as the LPF upper

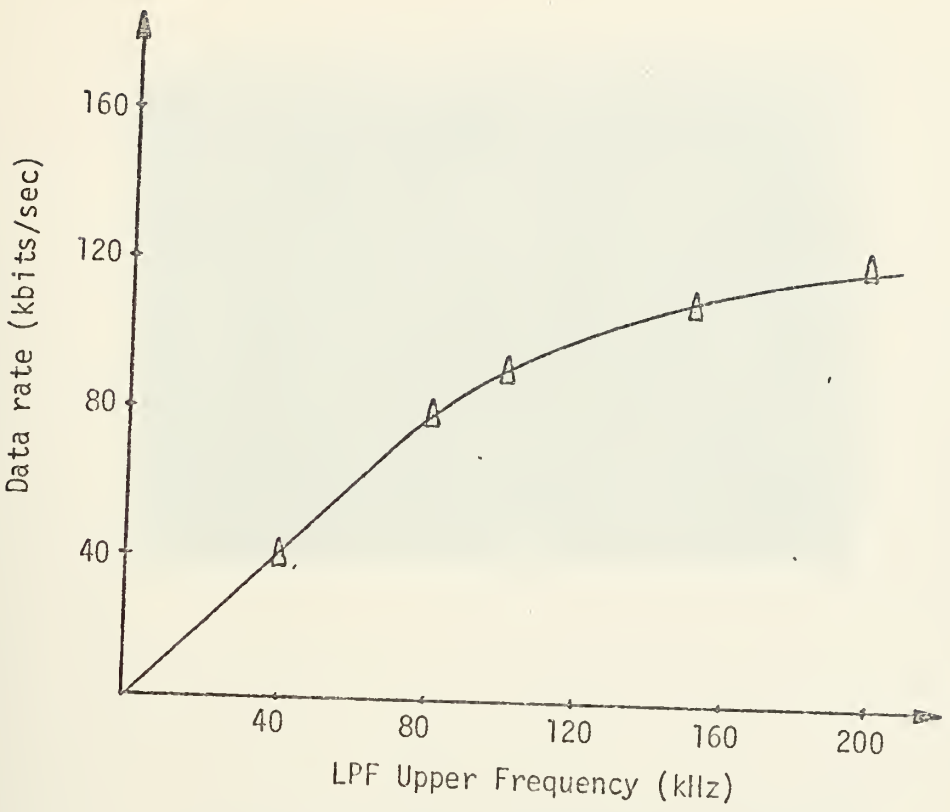


FIG. 22. DATA RATES VS. LPF UPPER FREQUENCY

frequency is increased the recovery of the modulating signal is enhanced. However as the increase is continued, high frequency terms begin to corrupt the recovered signal.

b. With Noise

The insertion of noise into the system complicates the task of analysis. It becomes necessary now to closely monitor the recovered signal, find techniques of comparing the recovered signal with the modulating signal and if discrepancies exist to count the number of such "errors".

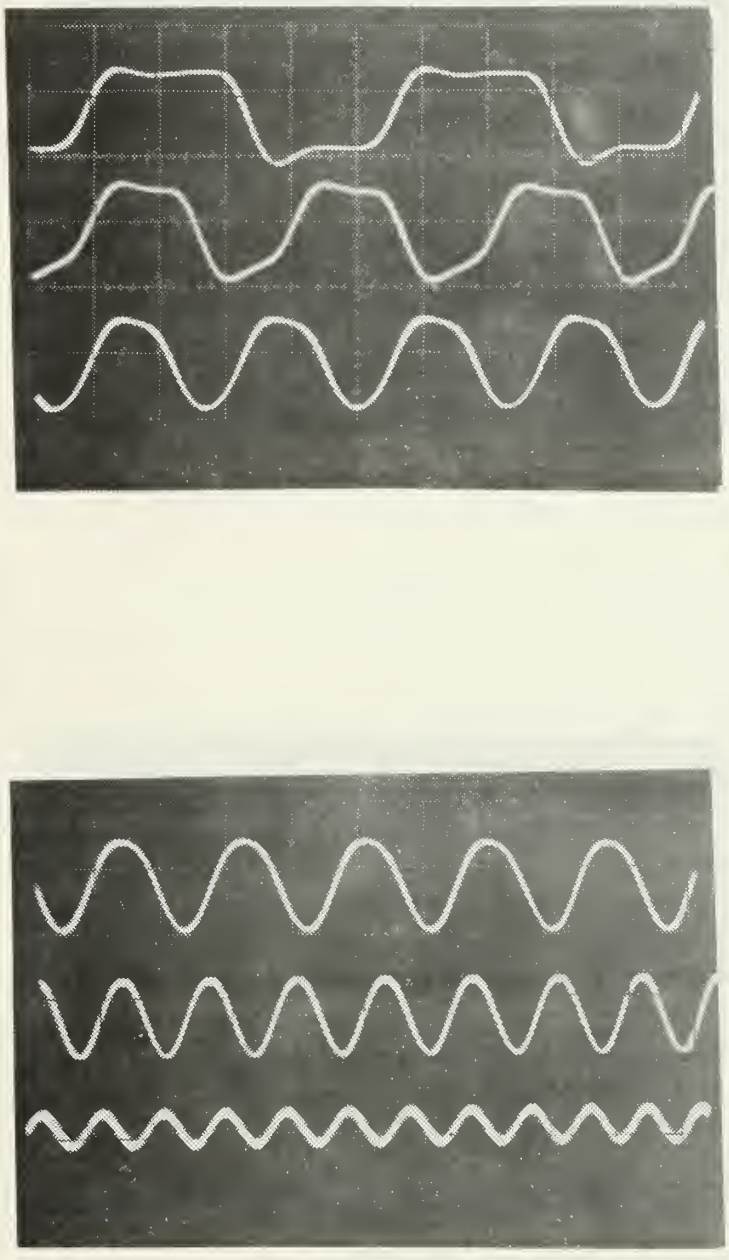


FIG. 23. THE EFFECT OF A CONSTANT LPF UPPER FREQUENCY ON THE RECOVERED SIGNAL IF THE DATA RATE IS CONTINUALLY INCREASED. Data rate increases from top to bottom.

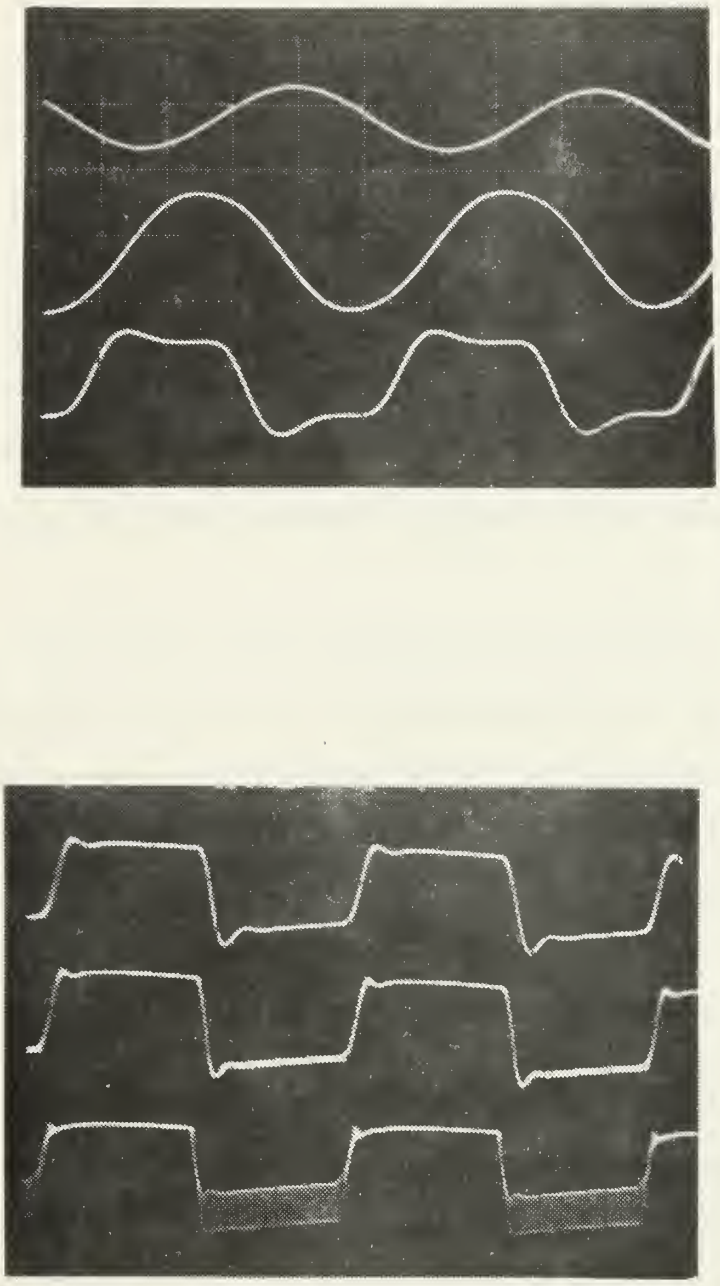


FIG. 24. THE EFFECT OF AN INCREASING LPF UPPER FREQUENCY ON THE RECOVERED SIGNAL AT A STEADY DATA RATE. LPF upper frequency increases top to bottom.

To accomplish this task the system of Fig. 25 is designed. Since many components of this system are frequency sensitive, it is necessary to select a data-rate range on which to base the design of this system. A data rate interval of 1.0 k bits/sec to 4 k bits/sec was selected. The system embodies four major subsystems which function to generate the necessary gating and timing pulses, recover the modulating signal, decide whether a "1" bit or a "0" bit was received and to count as errors any discrepancies which may exist in the comparison of the recovered signal with the modulating signal.

The error measurement gating circuit block diagram appears in Fig. 26. The purpose of this circuit is to generate a series of pulses which will constitute the basic timing sequence for all error measurement. Appendix A, Fig. 7, shows the schematic diagram of the error measurement gating circuit.

Figure 27 shows photographs of the waveforms generated by this circuit. The theory of operation is straightforward. Starting at a frequency which is twice the desired data rate, the waveform (a) is integrated (b) and applied to a threshold device which produces the waveform (c). The waveform (c) will constitute the "look time" in checking for the "1" or "0" bit. At the same time the starting frequency is applied to a frequency divider which produces waveform (d), the modulating signal. The frequency of waveform (d) also represents the data rate in use. The relationships of

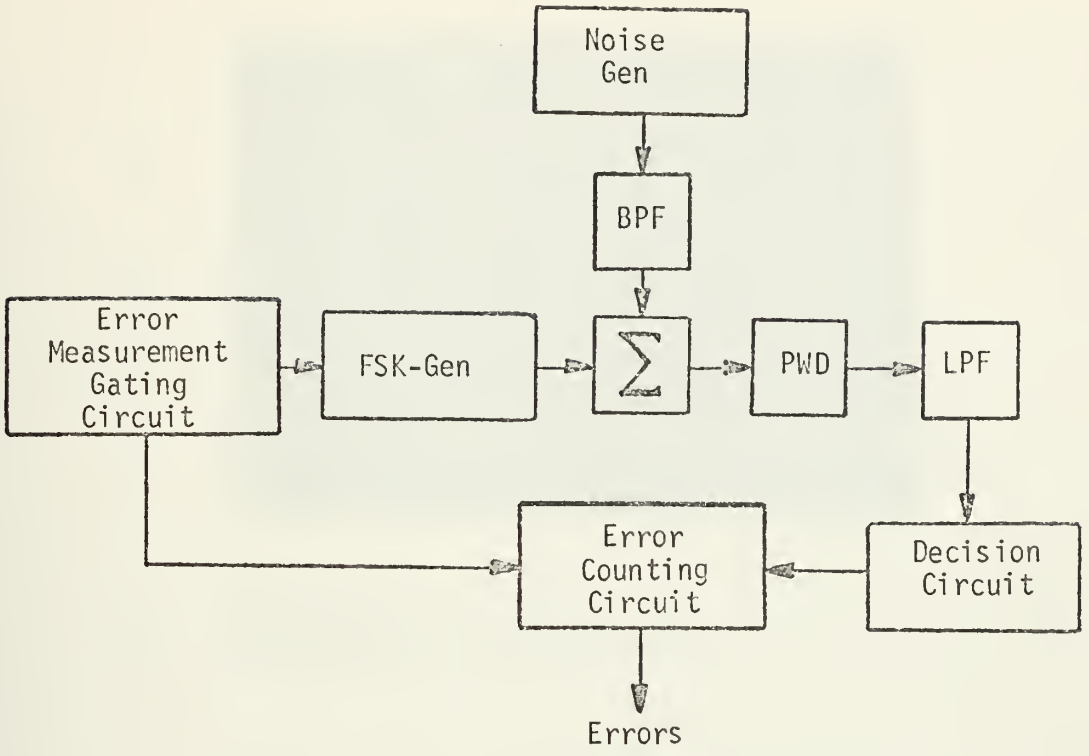


FIG. 25. BLOCK DIAGRAM OF A SYSTEM DESIGNED TO MEASURE ERRORS

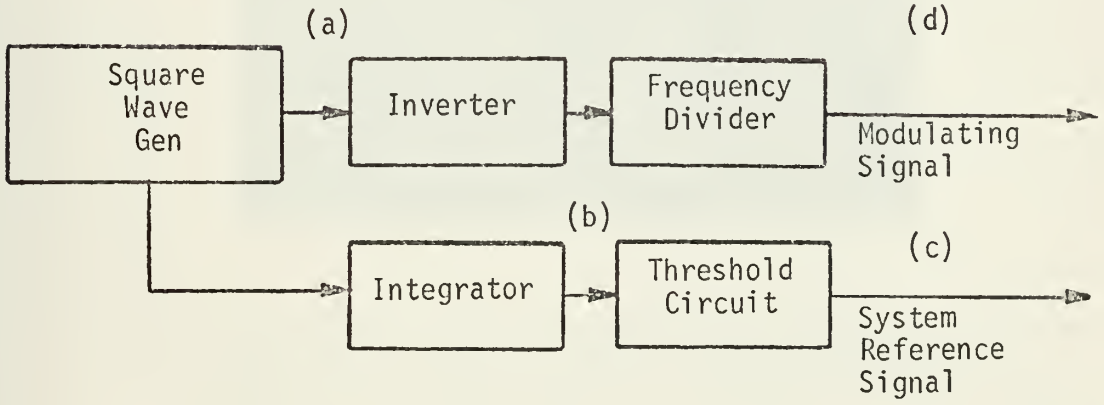
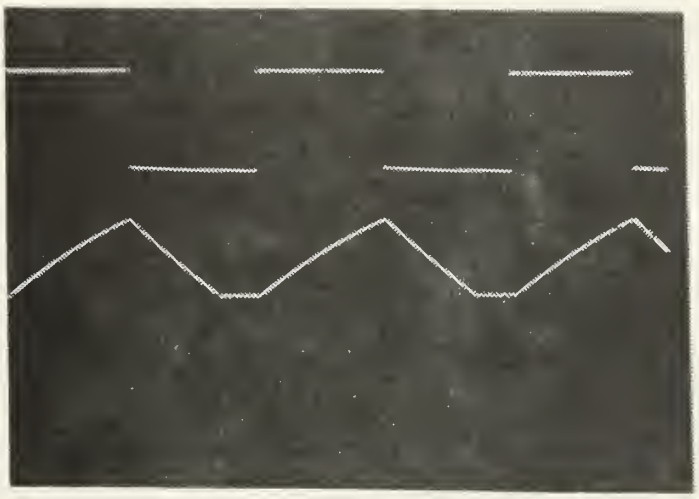


FIG. 26. BLOCK DIAGRAM OF THE ERROR MEASUREMENT GATING CIRCUIT

(a)

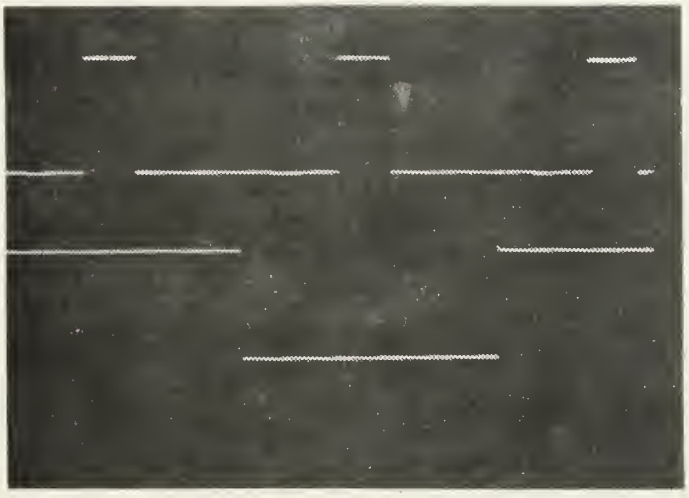
(b)



(a) Starting square wave.
(b) Integration of waveform (a).

(c)

(d)



(c) The output of the threshold circuit to which waveform (b) is applied. This waveform constitutes the timing reference for the error measurement system.
(d) The frequency divider output to which waveform (a) is applied. This waveform is the modulating signal used to produce the FSK signal.

FIG. 27. WAVEFORMS OF THE ERROR MEASUREMENT GATING CIRCUIT

waveforms (c) and (d) are very important because the presence of "1" or "0" bit will be tested for only during the interval of waveform (c).

The decision circuit is shown in Fig. 28. It consists of an integrator, an amplifier, an inverter and two threshold circuits. The schematic diagram of this system is found in Appendix A, Fig. 8.

The circuit receives the recovered waveform and integrates it to smooth out any noise induced amplitude fluctuations. The resultant wave is amplified and applied to a threshold circuit where a check is made for the presence of "1" bits. Simultaneously the recovered wave, after integration, is inverted and also applied to a threshold circuit where a check is made for the presence of "0" bits. The threshold circuits are identical and when triggered produce a pulse only if a "1" or "0" bit is detected.

Figure 28 shows that the decision circuit has two outputs. One output is a waveform which represents the presence of all "1" bits while the second output represents the presence of all "0" bits. The two waveforms are essentially identical except for a seemingly 180 degrees phase shift. This is true only because the modulating signal is a square wave rather than a sequence of pulses representing a code word.

Figure 29 shows the waveforms of the decision circuit when testing for the presence of "1" bits while Fig. 30 shows the waveforms when testing for "0" bits. It

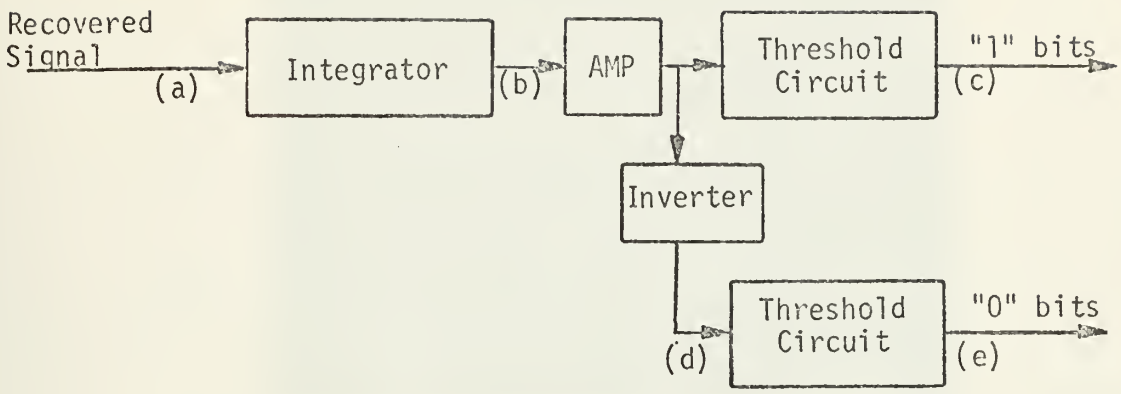
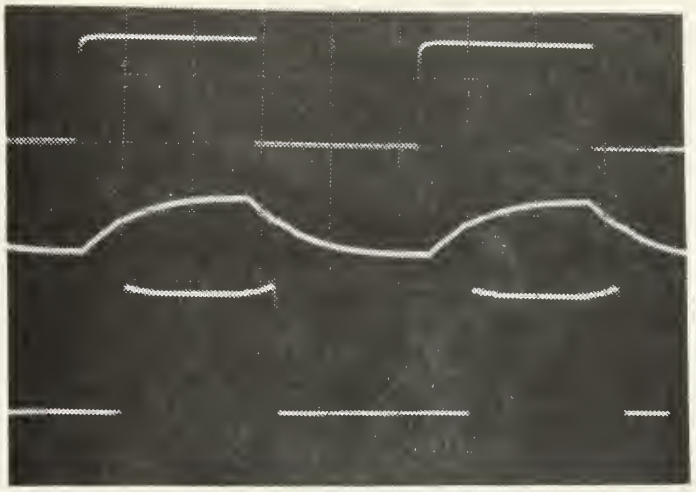


FIG. 28. THE DECISION CIRCUIT

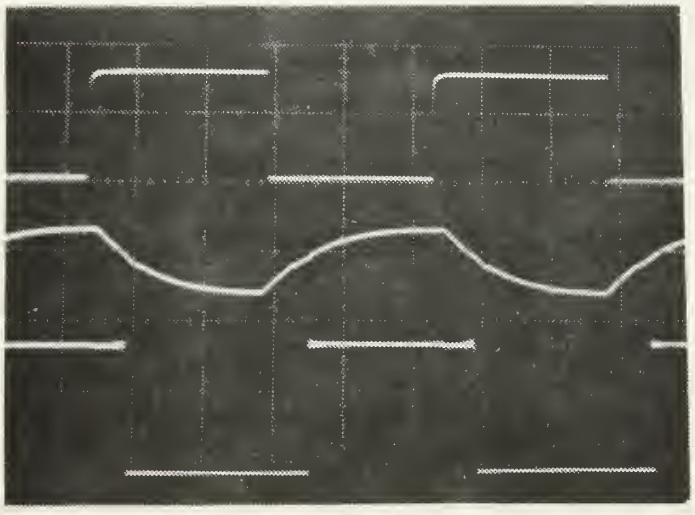
should be kept in mind that failure to trigger the threshold circuit will cause the respective "1" or "0" bit waveform to miss a pulse. When this occurs an error will be counted. The two outputs from the decision circuit, representing the "1" and "0" bit checks, proceed separately to the error counting circuit shown in Fig. 31.

At the error counting circuit the "1" and "0" bit waveforms from the decision circuit are now processed separately with a reference signal obtained from the gating circuit. This reference signal is waveform (c) of Fig. 27 and represents the position of the "1" and "0" bits of the original modulating signal (waveform (d) of Fig. 27). In the laboratory, waveform (c) is obtained by applying waveform (b) of Fig. 27 to a pulse generator. Obtaining the reference signal this way provides the needed flexibility of adjusting the reference signal delay time over very wide ranges. The



(a) A recovered "1" bit.
(b) Waveform (a) integrated.
(c) A new "1" bit generated by the threshold circuit.

FIG. 29. THE DECISION CIRCUIT WAVEFORMS FOR THE CASE FOR A "1" BIT INPUT



(a) A recovered "0" bit.
(d) Waveform (a) integrated.
(e) A new bit generated by the threshold circuit to mark the location of the "0" bits.

FIG. 30. THE DECISION CIRCUIT WAVEFORMS FOR THE CASE OF A "0" BIT INPUT

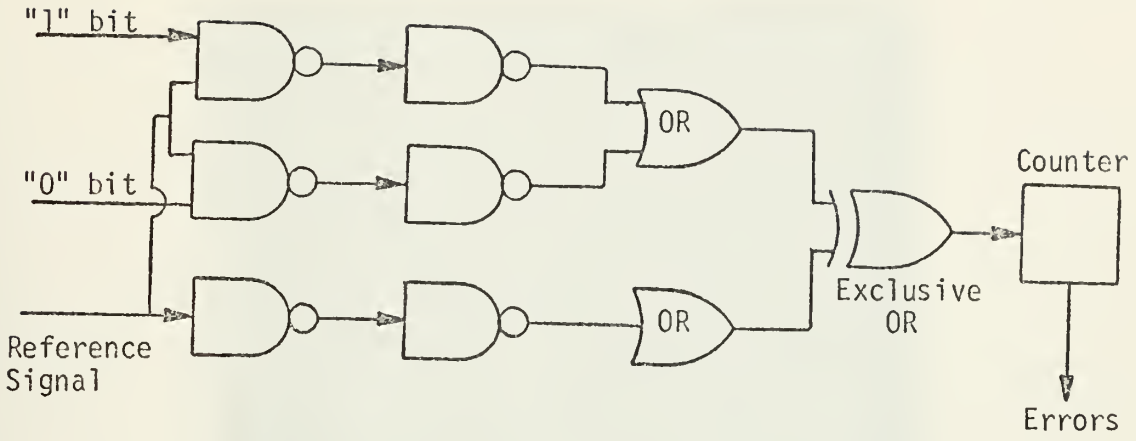
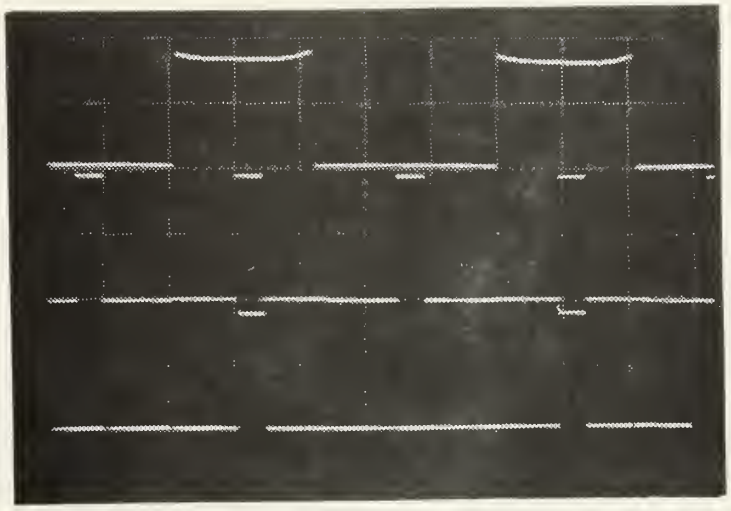


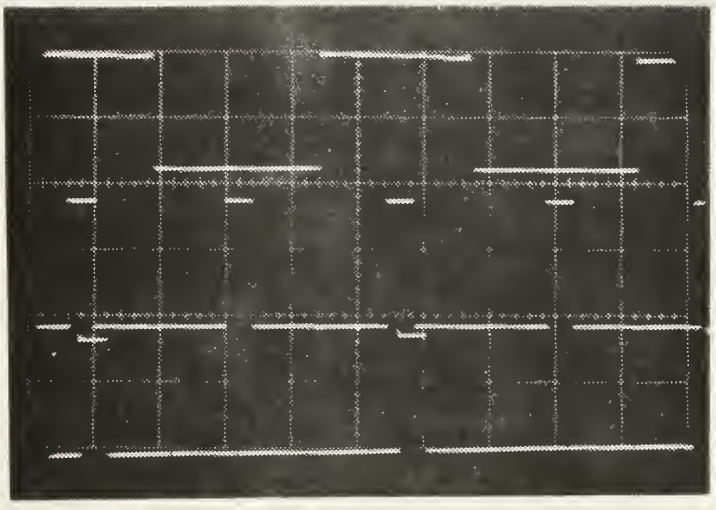
FIG. 31. THE ERROR COUNTING CIRCUIT

delay adjustments are necessary to place the reference signal precisely in the center of the "1" and "0" bit waveform produced by the decision circuit. The desired time relationship between the reference signal and "1" and "0" bit waveform from the decision circuit is the same as the relationship of waveforms (c) and (d) of Fig. 27.

The processing of the "1" and "0" bit waveforms with the reference signal is shown in Fig. 32 (a) and (b). Note that after processing, the location of the "1" and "0" bits is marked by the presence of a pulse identical to the reference pulse. The pulses denoting the position of the "1" bits (bottom waveform of (a)) and the pulses denoting the position of the "0" bits (bottom waveform of (b)) are now combined in an OR gate. The resultant waveform is identical to the reference waveform under conditions of no errors. Both waveforms are now applied to the exclusive OR. To insure



(a) The photograph indicates the processing applied to the "1" bit waveform (top) and the reference signal (middle). The result is the bottom wave form which signals the location of each "1" bit received.



(b) The photograph indicates the processing applied to the "0" bit waveform. Note that the bottom waveform signals the location of each "0" bit received.

FIG. 32. THE ERROR COUNTING CIRCUIT WAVEFORMS

the simultaneous arrival at the exclusive OR by both waveforms, the reference wave is routed through circuitry which is identical to the circuits which process the "1" and "0" bit waveforms.

It is seen that under conditions of no errors, the signals applied to the exclusive OR are identical. Therefore, there is no output from the exclusive OR. When an error occurs, and a "1" or "0" bit is missing, the exclusive OR input signals are not identical and a pulse is produced at the exclusive OR output. This pulse is then counted as an error.

With the system of Fig. 25 connected for operation, various levels of noise are added to the frequency modulated signal which is then applied to the PWD. The recovered signal is then compared to the modulating signal and all discrepancies are counted as errors. Simultaneously the SNR is computed from the rms noise and signal measurements taken at the output of the summing amplifier. The resultant error rates are plotted on the theoretical curve for the probability of error versus SNR (dB) for a non-coherent FSK system [Ref. 5]. The results are shown in Fig. 33. Note that the experimental results are in good agreement with theory.

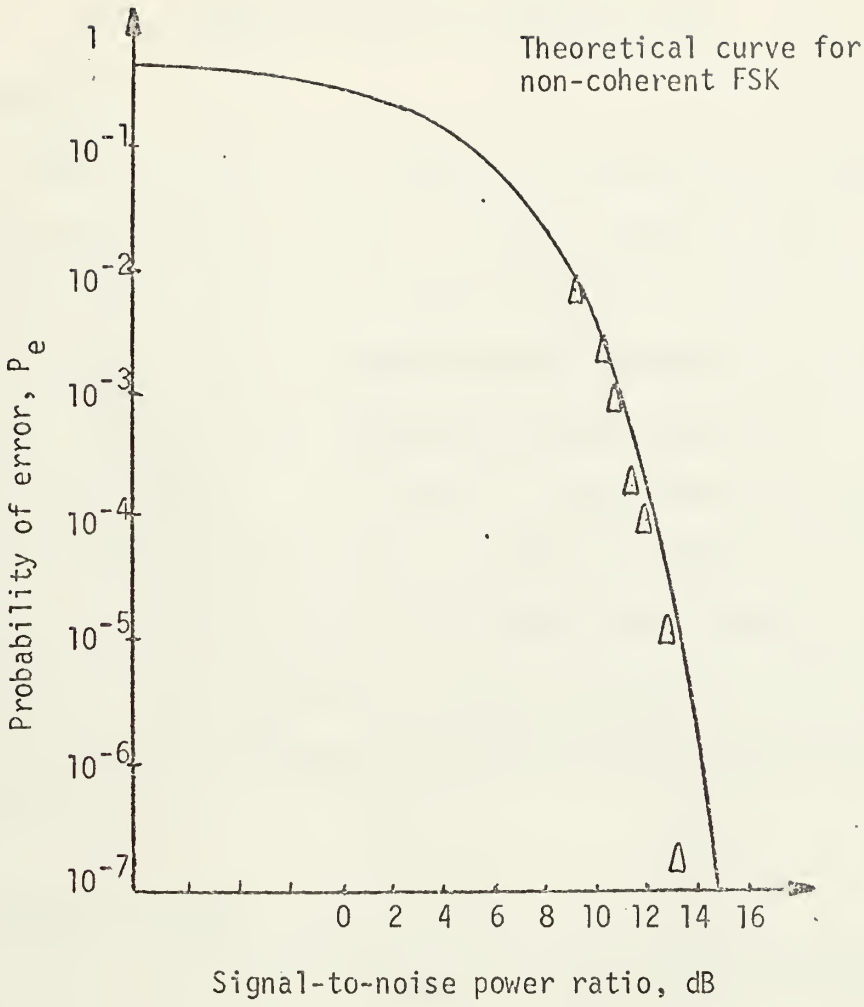


FIG. 33. PROBABILITY OF ERROR VS SNR FOR A NON-COHERENT FSK SYSTEM. Data points obtained in the laboratory are shown as triangles.

IV. SUMMARY AND RECOMMENDATIONS

A. SUMMARY

It seems likely that digital frequency demodulators will become increasingly popular. These devices offer advantages in economy and quality of performance over their analog counterparts. Digital demodulators function well with analog or digital (FSK) input signals at both commercial intermediate frequencies (455 kHz, 10.7 MHz). When noise is introduced, the PWD recovers good quality sound at SNR of 9.5 dB. Similarly, when noise and FSK signals are applied, the demodulator functions well producing error rates which are in agreement with theoretical predictions for non-coherent FSK systems.

B. RECOMMENDATIONS

To improve the performance of digital demodulators it is necessary to fabricate the device-limiter and demodulator on a single chip. The benefits so derived will be lower circuit noise and reduced vulnerability to ambient noise. Circuit noise appears to be the major factor in determining the minimum frequency deviation necessary to insure the recovery of a strong signal.

APPENDIX A

Appendix A presents the schematic diagrams of all the circuits used throughout this investigation. The components used to implement the various systems include NAND gates, OR gates, exclusive OR gates, JK flip flops, operational amplifiers, Schmitt triggers and the monostable multivibrator. Detailed information (operating characteristics) for each component are found in Refs. 6 and 7. The values of all resistors are in k (10^3) ohms while the capacitors are in micro (10^{-6}) farads unless otherwise indicated.

The various circuit diagrams are presented in Figs. A-1 through A-8 in the following order:

Fig. A-1. The Hard Limiter
Fig. A-2. PWD and the Delay Line
Fig. A-3. 50 dB Amplifier
Fig. A-4. Pulse Shaping Circuit
Fig. A-5. Summing Amplifier
Fig. A-6. Saturating Amplifier and Schmitt Trigger
Fig. A-7. Error Measurement Gating Circuit
Fig. A-8. Decision Circuit

Figure A-1 shows the limiter which appears in Fig. 4. The output of the limiter must be a negative going pulse (4 volts to 0 volts) to properly trigger the pulse circuit.

Figure A-2 shows the PWD and the NAND gate delay line (approximately 100 nsec) which appears in Fig. 9. The delay line improves the PWD performance at high frequencies.

Figure A-3 is the schematic diagram of the 50 dB amplifier of Fig. 15.

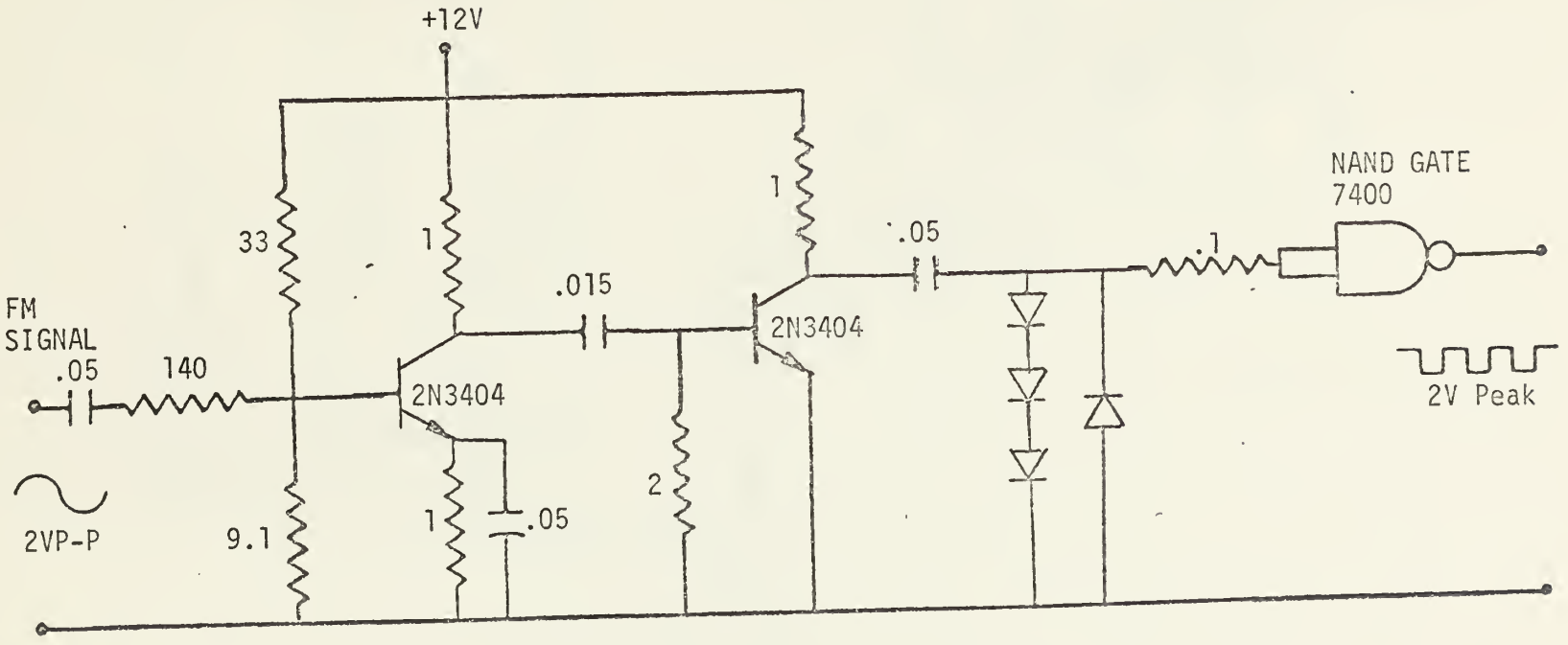
Figure A-4 shows the schematic diagram of the pulse shaping circuit which is used for the recovery of digital modulating signals. The circuit consists of a zero crossing detector which produces 4 volt pulses to simplify the comparison of the recovered and the modulating signals. Figure 21 shows its location in the system.

Figure A-5 presents the summing amplifier schematic diagram first introduced in Fig. 16. The summing amplifier is necessary when noise is added the the frequency modulated signal. The amplifier provides a gain of 10 dB to both inputs (noise and FM signal). The amplitude of the FM signal at the input to the summing amplifier must be 0.2 volts or less to maintain linear operation.

Figure A-6 shows the schematic diagram of the saturating amplifier and the Schmitt trigger which appears in Fig. 17. This circuit receives the normal 2 volt peak-to-peak output from the summing amplifier and produces a 4 volt pulse waveform which is then applied to the demodulator. The presence of the saturating amplifier and Schmitt trigger obviates the need for the PWD limiter. However, since the limiter and the PWD were fabricated on a printed circuit board, it was allowed to remain. The initial vulnerability of the PWD to noise was because the limiter was designed to limit at approximately zero volts. Subsequent addition of the Schmitt trigger to the system replaced the zero threshold operation resulting in acceptable PWD performance under conditions of additive noise.

Figure A-7 presents the schematic diagram of the error measurement gating circuit which appears in Fig. 26 in block diagram form. The circuit produces two waveforms: (1) the modulating signal and (2) the error measurement gating signal. The waveforms produced by this circuit are shown in Fig. 27 (c) and (d). Figure A-7 shows that a ±2.5 volt square wave is clamped to 0 volt level (bipolar converted to unipolar) and is used to trigger a NAND gate which in turn produces the standard 4 volt pulse used by the PWD. Two NAND gates are used to obtain the original polarity of the initial square wave. This signal is applied to an amplifier which drives the frequency divider (JK Flip Flop), and to an integrator which produces a sawtooth waveform. The output of the frequency divider is applied to another driver which has a resistive divider network as its load. The output of the divider network is the modulating signal and is approximately 40 mV in amplitude. This signal is now routed to the sine wave generator to modulate the carrier. The integrator output is used to trigger a pulse generator (Data Pulse 101 Pulse Generator) which is capable of continuous adjustment of its output parameters (amplitude, width and delay).

Figure A-8 is the schematic diagram of the decision circuit shown in Fig. 28. The amplifiers of Fig. A-8 are from left to right: integrator, amplifier and comparator. The bottom row amplifiers are an inverter and a comparator. The circuit waveforms are shown in Fig. 30.



All resistors in k ohms
All capacitors in μf
All diodes are silicon type

FIG. A-1. THE HARD LIMITER

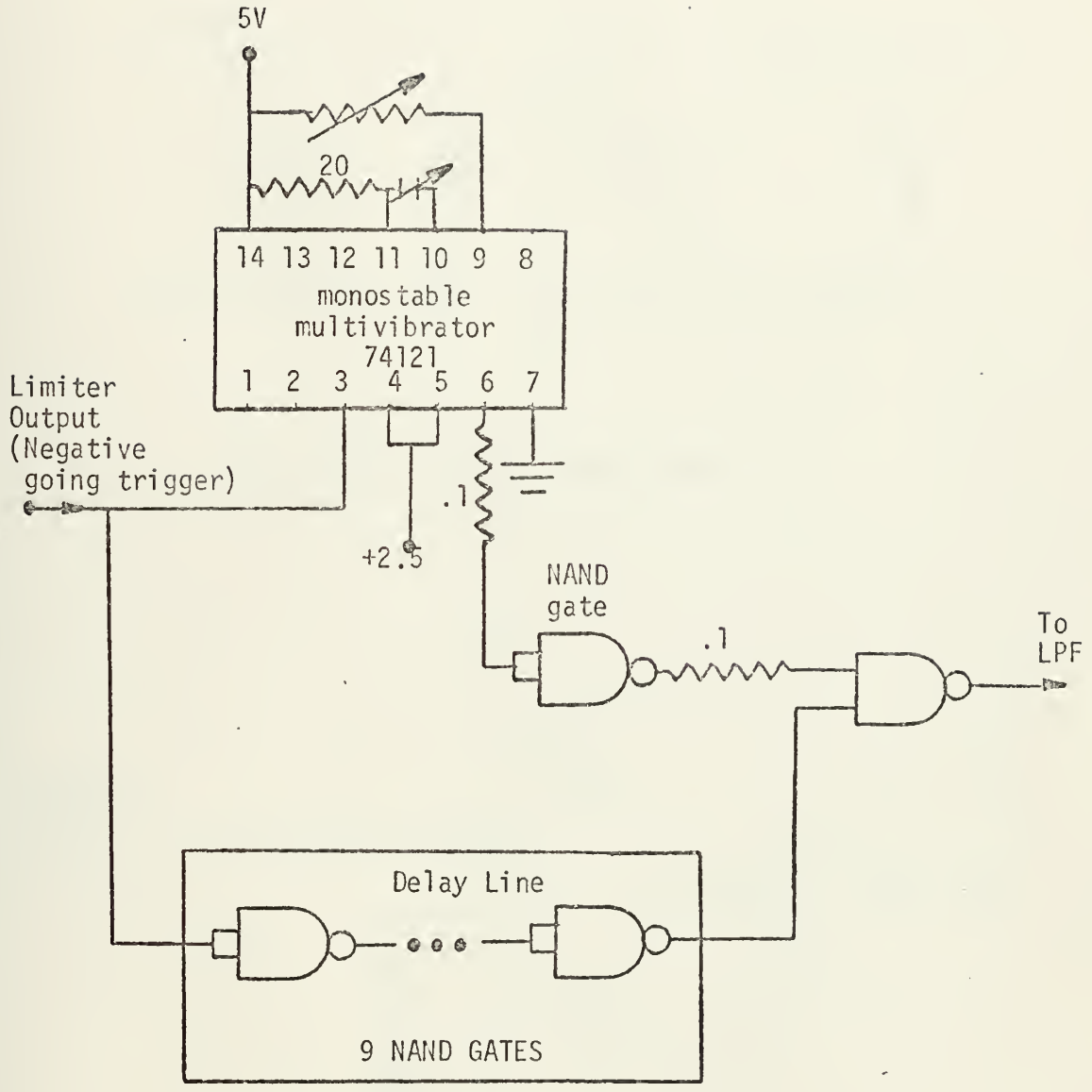


FIG. A-2. PWD AND DELAY LINE

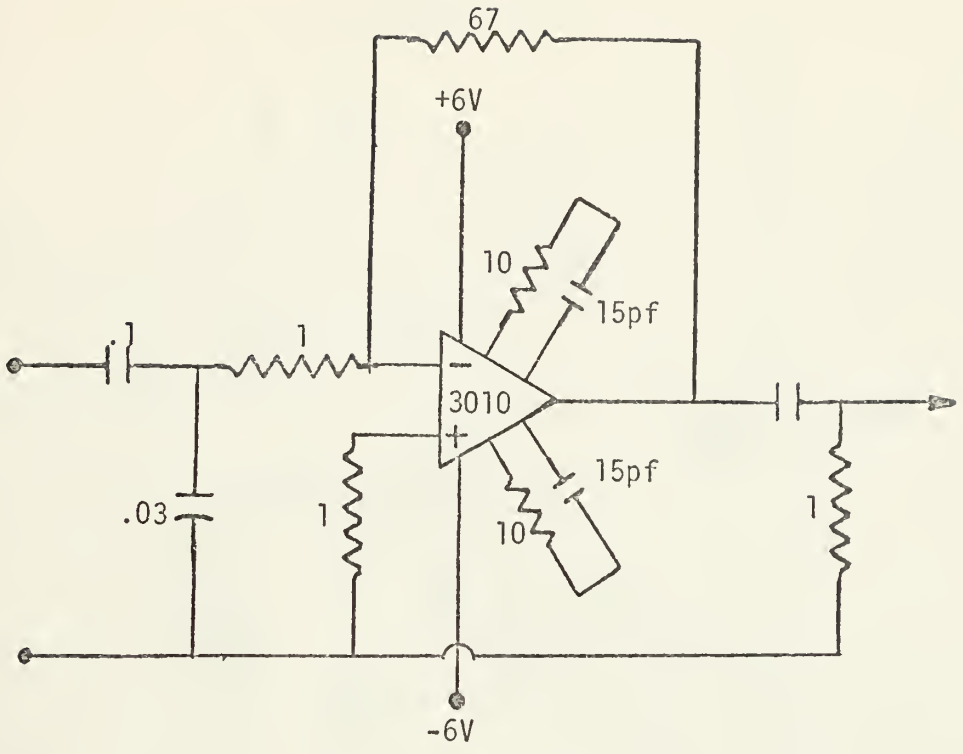


FIG. A-3. 50 dB AMPLIFIER

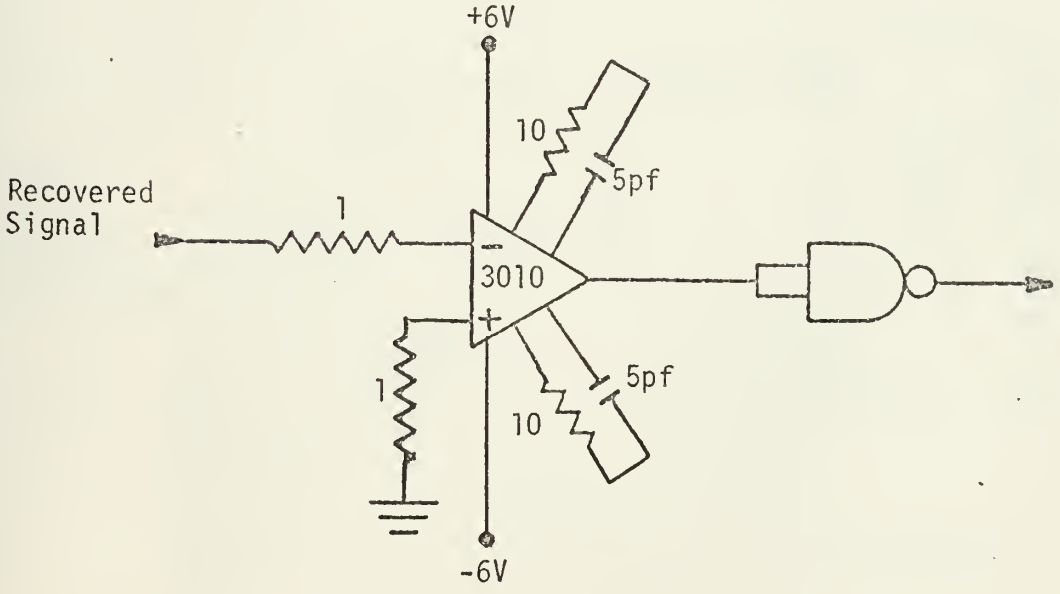


FIG. A-4. PULSE SHAPING CIRCUIT (ZERO CROSSING DETECTOR)

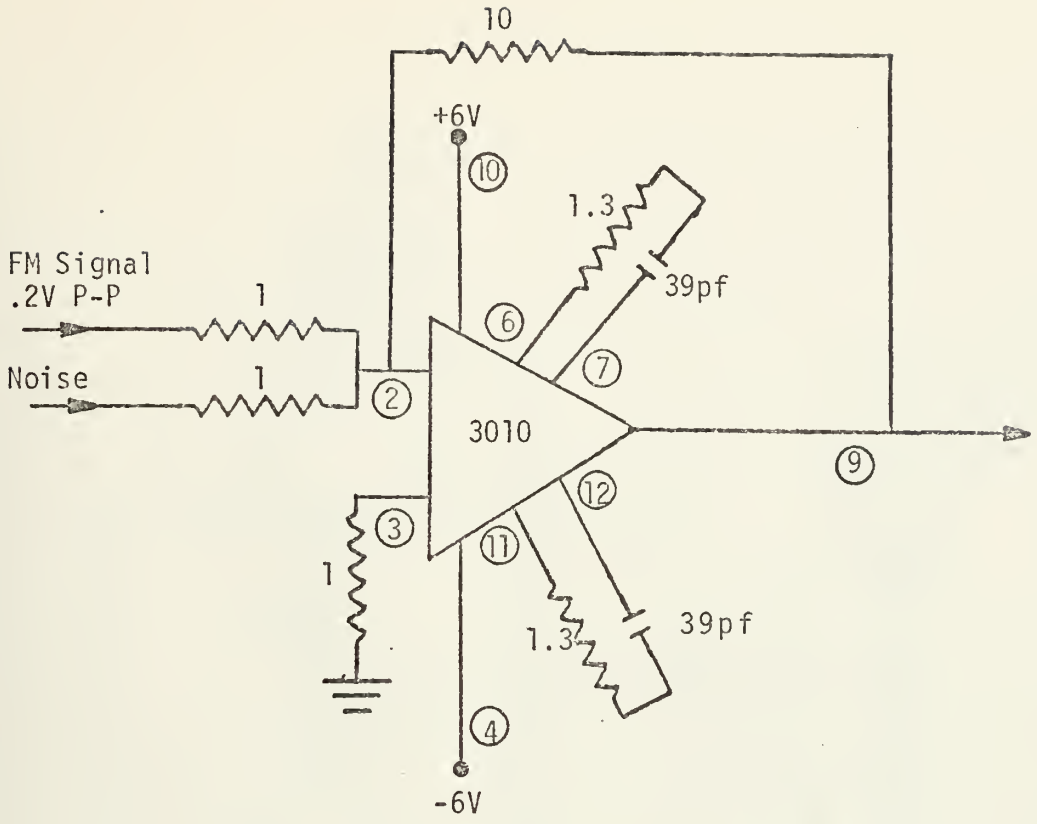


FIG. A-5. SUMMING AMPLIFIER

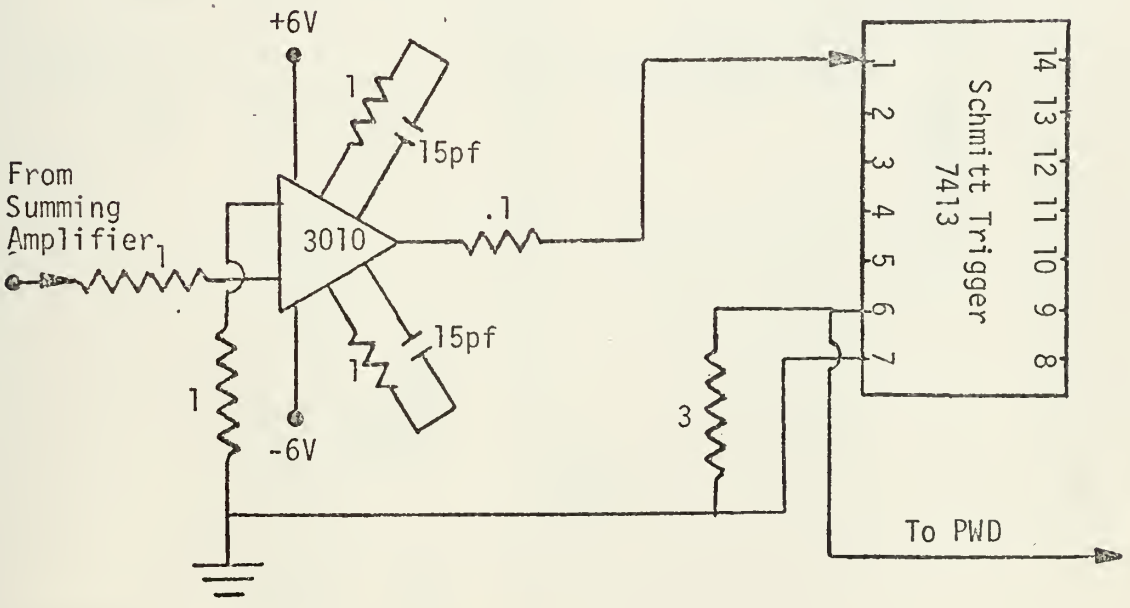


FIG. A-6. SATURATING AMPLIFIER AND SCHMITT TRIGGER

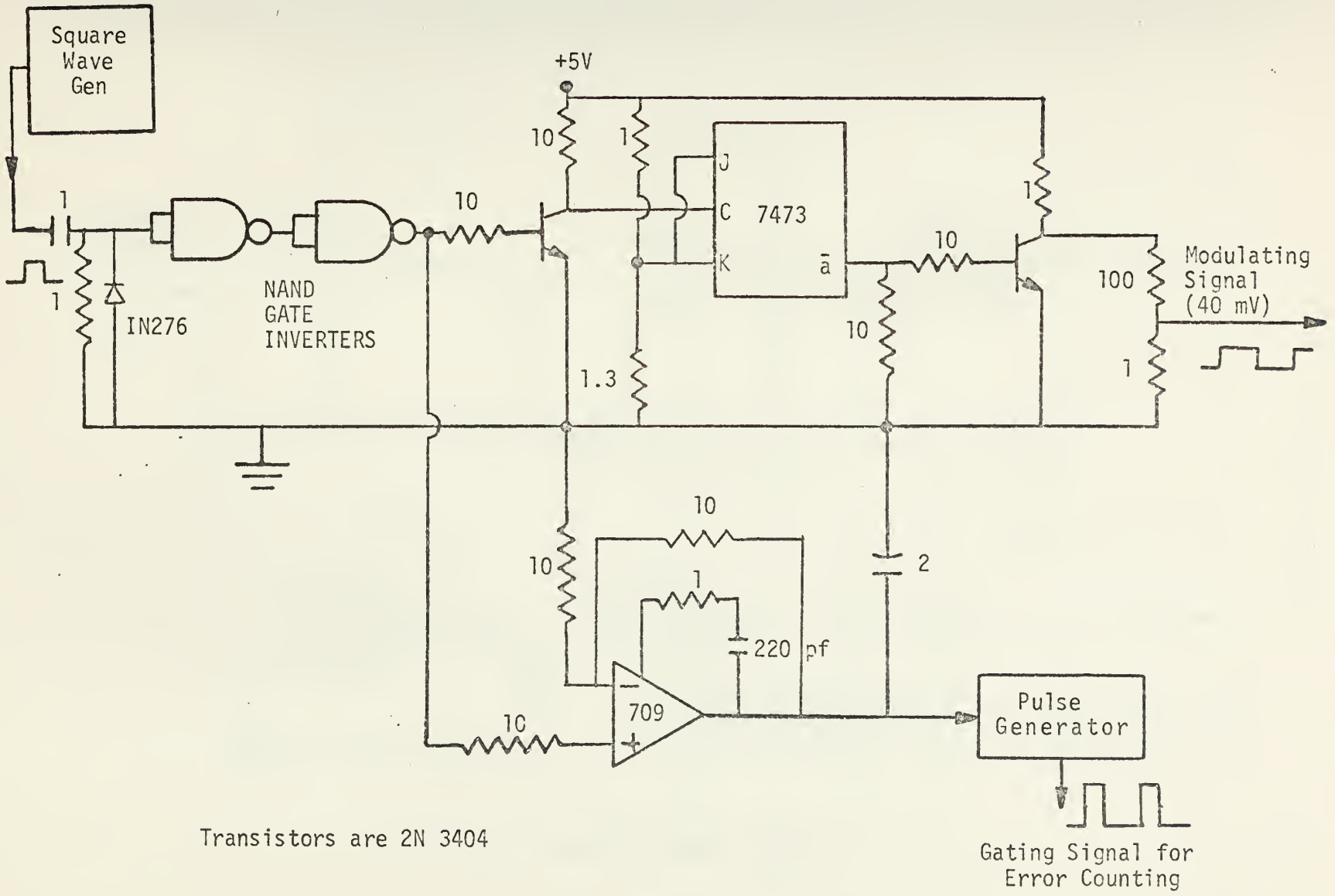


FIG. A-7. ERROR MEASUREMENT GATING CIRCUIT

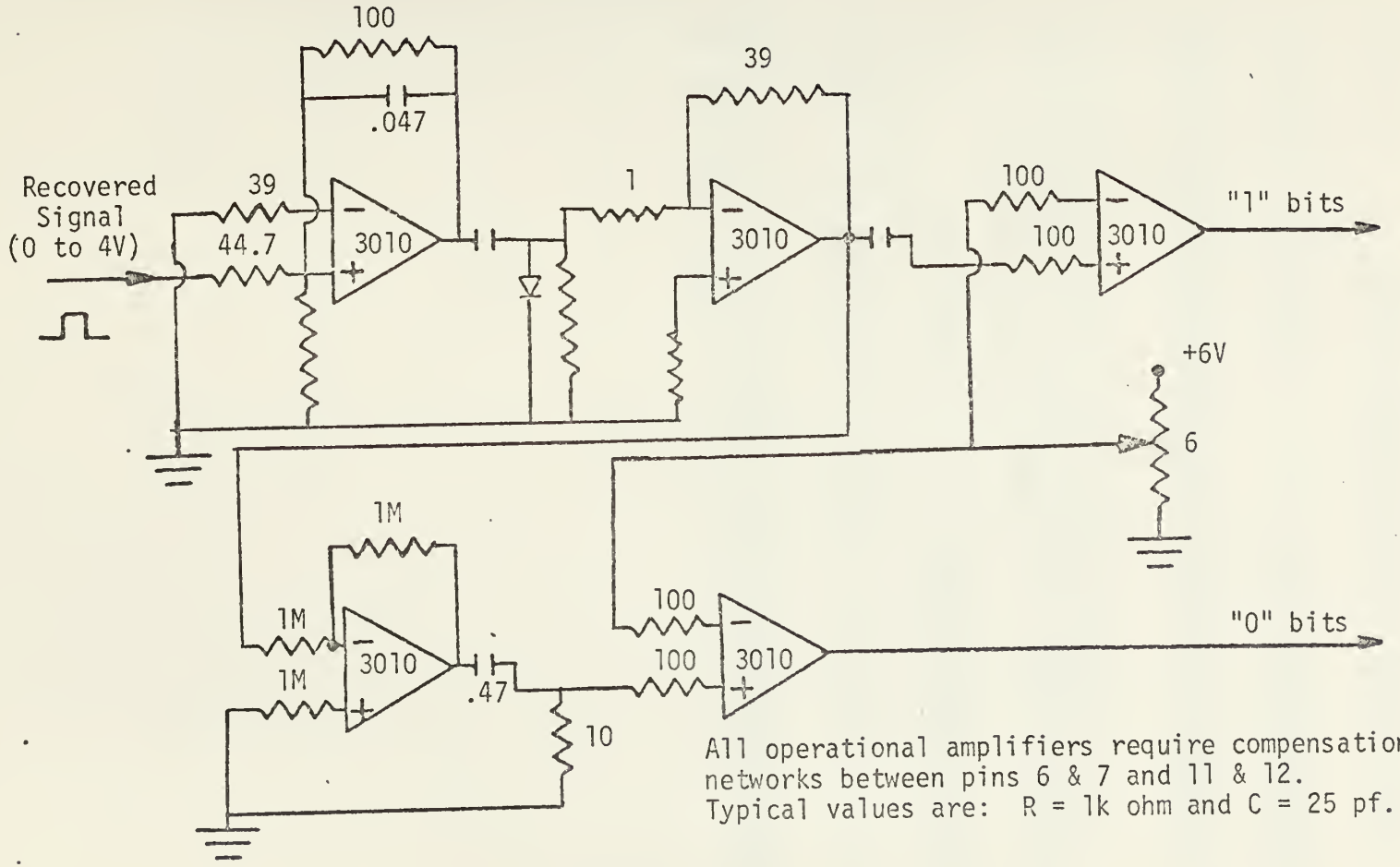


FIG. A-8. THE DECISION CIRCUIT

LIST OF REFERENCES

1. Terman, F.E., Electronic and Radio Engineering, Fourth Edition, p. 605-614, McGraw-Hill, 1955.

2. Clark, K.K. and Hess, D.T., Communication Circuits: Analysis and Design, p. 571-625, Addison-Wesley, 1971.

3. Hewlett-Packard Journal, A Wideband Analog Frequency Meter and FM Discriminator, Volume 18, Number 7, March 1967.

4. Garodnick, J., Greco, J., and Schilling, D.L., "Theory of Operation and Design of an All Digital FM Discriminator," IEEE Transactions on Communications, p. 1159-1165, December, 1972.

5. Stein, S., and Jones, J.J., Modern Communication Principles, p. 221-241, McGraw-Hill, 1967.

6. Signetics, Integrated Circuits, Data Book, p. 2-2, 2-6, 2-68, 2-117, 1974.

7. RCA Solid State Databook Series, Linear Integrated Circuits and MOS Devices, Application Notes, (SSD-202A), p. 262-276, 1973.

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